Abstract—Digital power amplifiers (DPAs) provide an unprecedented level of flexibility in their ability to operate on different signals using simple reprogramming of the DSP, but their output matching networks must be redesigned for different frequency bands. This involves a redesign of part of the back-end-of-line (BEOL) mask set at great cost. We present a package level reconfiguration technique that allows a single transmitter to be reconfigured for multiple frequency bands, or different output power levels by soldering different SMD components directly to the surface of the die, saving design and fabrication cost while delivering similar performance. We demonstrate the technique on a multiphase transmitter IC, showing optimized operation at three different frequencies using soldered SMD components to reconfigure the matching network of the IC at the package level. The transmitter’s linearity and performance are validated using a 5MHz, 64QAM LTE signal.

Index Terms— Reconfigurable RF Circuits, Package Level SMD Integration, Digital Transmitter, SCPA, RF Matching Networks

I. INTRODUCTION

There is great interest in reconfigurability in RF circuits at to support software-defined/cognitive radio and also to decrease non-recoverable engineering costs associated with optimizing wireless front-ends for differing frequency bands. Digital power amplifiers (DPAs) and transmitters provide flexibility in their ability to interface directly with DSP while providing broadband linear outputs. DPAs using transistors as unit current cells [1]–[5], resistors [6], [7] and switched-capacitors have been presented [8]–[10]. There are few solutions for RF reconfigurability. Present solutions use either on-chip matching networks (e.g., MIM capacitors and spiral inductors), or off-chip surface mount devices (e.g., SMD inductors and capacitors) for impedance transformation. In the former case, large chip area is incurred to allow for multi-band operation, as separate matching networks are required for each frequency [11]; additionally on-chip matching networks are subject to large losses owing to their relatively low component quality factors [12]. In the latter case, off-chip passives must be used at the expense of placement/manufacturing cost and increased surface area used on the printed circuit board [13], [14].

Recently, efforts to allow reconfigurability for low-and high-power transmit modes have been incorporated using high voltage switched-capacitor circuits [15]. This method allows for modulation of the load impedance, which can be used to enable/disable high- and low-power modes, but offers little control of the operation frequency. Furthermore, the switches used incur large area and add significant parasitics leading to additional losses. Incorporating a switch in the inductor path would allow more flexibility in the ability to control the frequency; however, switching the inductors adds even more prohibitive losses, as the quality factor of the inductors is severely degraded by the presence of a switch.

Recently, efforts have been made to integrate passives into the PCB [16], or as SMDs bonded directly on the integrated circuit die [17]. In both cases, the goal was to provide a high quality passive with reduced footprint on the integrated circuit die and the PCB. These demonstrations were for DC-DC converters used for power management ICs (PMICs); PMICs have reduced tolerance to losses when compared with RF circuitry. Hence, the approaches are also applicable for RFIC applications. Because the PCB integration results in larger inductances and hence, reduced operating frequency, we propose to integrate package level reconfigurable matching networks on chip using multi-component SMD matching networks, as shown in Fig. 1.

SMD passives have several key advantages when compared to on-chip planar spirals. First, the passives are farther away from the silicon substrate, subjecting them to lower coupling.
via the electric and magnetic fields. Second, the geometry of the inductor can be chosen to reduce lateral eddy currents that are typically induced in the silicon substrate. Finally, the size constraints are reduced; inductors of 10’s of nH and capacitors of 100’s of pF can be easily realized in 10×20 mil packages. In this paper we present a package level reconfiguration technique using SMD components that can be easily optimized for frequency and output power level at time of final assembly, allowing die reuse, allowing for significant cost saving in reconfiguration. Though the matching networks are not field reconfigurable, they are able to be reconfigured at the package level. This is considerably cheaper than back-end-of-line (BEOL) mask changes which would be necessary to reconfigure an integrated passive matching network and can be accomplished using parasitic aware circuit simulations coupled to 3-D EM simulations. Additionally, space savings can be achieved in technologies that allow for circuit-under-pad (CUP) designs.

The paper is organized as follows. First, we detail the SMD on package techniques in Section II. In section III, we detail applications in a digital transmitter. Measurement results for several configurations are presented in Section IV, followed by conclusions in Section V.

II. SMD ON CHIP PACKAGING

Modern CMOS processes typically consist of 8-10 metal layers and interface with the package using wirebonding or flip-chip via a thick aluminum top metal layer. In principle, it is possible to solder directly to aluminum if the temperature, solder material and flux selection are optimal; in practice, at chip scale it is difficult to achieve the right combination of processing and ingredients to enable this.

A. Gold Stud Bumping

In order to accommodate SMD components directly on chip, we have opted to place eutectic bonded gold studs directly on the IC bondpad [18]. This process utilizes the same techniques used for standard wirebonds and can be performed at the same time as wirebonding and packaging. It should be noted that wirebond pads typically do not allow placement of circuits underneath the pads due to mechanical stresses. Due to the large size of the pads, this can use substantial chip area. However, in more recent CMOS processes there are options for CUP design that allow area savings. In order to minimize contact resistance, the packaging assembler should place as many gold studs as possible on the pads. An example gold-stud bumping pattern for three 10×20 mil SMD components is shown in Fig. 2. Note that each pad is able to accommodate 12, 75µm diameter gold bumps. There are also increasingly options for smaller SMD components (e.g. 5×10 mil, etc.).

B. Solder Paste Assembly

Upon completion of the gold stud bonding procedure, SMD components can be attached to the stud bumps using a number of soldering materials. Many of the typical soldering materials embrittle gold and hence the quality and lifetime of the soldering joint can be reduced. Leadless solders have reduced reliability due to fatigue and hence should be avoided. In our design we have chosen to use a Sn-Ag-Cu paste which shows higher reliability and reduced fatigue [19]. If fatigue is an issue, Indium alloys (e.g., In70Pb30) are suitable, however with lower thermal tolerance. Using a Sn-Ag-Cu paste, the paste is placed directly on the gold stud bumps using a micropositioner. Following this, the SMD components are reflowed in an oven with a temperature profile optimized for the Sn-Ag-Cu solder.

Due to the solder choice, the process is not repeatable, as an attempt to reflow the components will result in removal of the gold stud bumps. Solders that do not embrittle the gold allow for the possibility of reworking the design. It is noted that this allows one transmitter to be designed and optimized for different frequency bands at the package level, before sealing of the package, offering cost savings. Neither the front-end-of-line, nor back-end-of-line metal needs to be altered; hence no mask redesign is needed to accommodate the operation. Care should be taken in spacing of the components to avoid unintentional short circuits. Margin should be added to the recommended spacing from the SMD manufacturer, as the gold stud bumps do not allow the solder paste to sit flat on the surface. In the displayed design (Fig. 2, Fig. 5), a margin of 2 times the recommended spacing from pad-to-pad was used to prevent solder bridging.

III. APPLICATION IN A MULTIPHASE TRANSMITTER

A. Switched Capacitor PA Design

A switched capacitor PA (SCPA, Fig. 3) is a special type of class-D PA, where the capacitive element in the series resonant output filter is sub-divided. All capacitors share a common top-plate connection toward the load; the bottom plates are driven by independently controlled CMOS inverters, acting as high- and low-side switches. This allows linear voltage amplitude control, by precisely controlling charge redistribution across the array of capacitors.

When all capacitors are switched at the RF center frequency,
The output power, $P_O$, of the SCPA:

$$P_O = \frac{1}{2} \pi \frac{(n)^2}{N^2} V_{DD}^2 R_{opt},$$

(1)

where $V_{DD}$ is the amplifier supply voltage, $n$ is the number of capacitors being switched, $N$ is the total number of capacitors and $R_{opt}$ is the optimal termination resistance. For full power, $n=N$, the output power is set by choosing $R_{opt}$.

The input power is the power required to switch the capacitors. It can be shown that the input capacitance, $C_{in}$ is given by the following [8]:

$$C_{in} = \frac{n(N-n)}{N^2} C_U.$$

(2)

The input power, $P_i$, is thus:

$$P_i = \frac{1}{2} C_{in} f_0 V_{DD}^2.$$

(3)

The efficiency is thus given by the following:

$$PAE = \frac{P_O}{P_O + P_i} = \frac{4\pi^2}{4\pi^2 + \pi^2 (N-n)^2 / N^2}.$$

(4)

where $Q_{nw}$ is the quality factor of the output network and is given by the following:

$$Q_{nw} = (2\pi f_0 C_{in} R_{opt})^{-1}.$$

(5)

Hence it can be seen that minimizing $C_{in}$ increases the PAE for all values of $n$. However, there are two competing goals to minimizing $C_{in}$. First, resolution is increased by sub-dividing the capacitor. Because there is a limit to the minimum size of capacitors available in a given process, the minimum size of the total capacitance is limited. Second, choosing a large $Q_{nw}$ results in more losses in the matching network that is used to transform the impedance and hence results in lower PAE [12], [20].

**B. Multiphase SCPAs**

SCPAs are polar transmitters that operate to combine the instantaneous amplitude and phase of a modulated signal, rather than to linearly amplify the signal. Because the operators that create the amplitude and phase are strongly non-linear, the resulting amplitude and phase modulation occupy significantly larger bandwidth than the linear signal. This means that the amplitude and phase modulation paths require significantly larger bandwidth (e.g. 5-10× the RF bandwidth). Furthermore the amplitude and phase paths require precise synchronization when they are combined at the SCPAs input. It has been shown that the synchronization must be < 5% of the symbol period of the modulation to maintain appropriate fidelity [21].

A quadrature SCPA (Q-SCPA) avoids the problems of bandwidth expansion and synchronization at the expense of reduced output power and efficiency [20]. For this reason, we have chosen to validate the performance of the reconfigurable matching networks using a multiphase SCPA (MP-SCPA)[10]. The MP-SCPA is a digital transmitter that uses amplitude weighting and phase interpolation to linearly and efficiently transmit non-constant envelope modulation.
In an MP-SCPA (Fig. 4), control logic, a switch and a capacitor are segmented into a tile of unit cells such that the control logic and switch interface with the bottom plate of a capacitor and the top plates of all of the capacitors are interconnected in an array. To provide coarse phase modulation, evenly spaced phases (e.g., $\phi_1-\phi_N$). Phase selection logic selects the two adjacent phases ($\phi_A-\phi_B$) to the desired output and distributes those phases to the tiled capacitor array through a chain of symmetric clock buffers. Though in our implementation the phase generation is performed off-chip, it can be performed on-chip with a PLL/DLL or a polyphasor filter. Both of the adjacent phases are routed to every cell in the array.

The control logic at the cell selects whether to switch the cell on $\phi_A$, switch on $\phi_B$, or hold the cell at ground. In this way, the output can be precisely controlled to interpolate the output phase of the array and the amplitude is controlled by selecting how many total cells are being switched (e.g., the fewer cells held at ground, the higher the output amplitude). Using more phases decreases the separation between the adjacent phases; hence when the phases are summed the output amplitude is larger and operates more efficiently.

The MP-SCPA presents a capacitive reactance at its output that is the sum of all of the unit capacitors in parallel. This is matched using inductors $L_1$ and $L_2$ ($C_1$ is a fixed on-chip MiM capacitor, sized to help control the loaded quality factor of the network). Because the reactance changes relatively constantly with frequency, the sizes of $L_1$ and $L_2$ only need be adjusted to allow control of the value of $R_{opt}$ (i.e., output power), or to control the output frequency at which the transmitter is tuned.

IV. MEASUREMENT RESULTS

An experimental prototype of the MP-SCPA with the package level reconfigurable matching network is fabricated in a 130nm RF CMOS process with an ultra-thick top metal. A chip microphotograph of the assembled transmitter is shown in Fig. 5. A comparison to a completely integrated design can be made from the figure; the lower right hand corner of the IC implements the same circuit with a fixed, completely integrated matching network.

The transmitter’s output power and power added efficiency (PAE) are measured versus frequency and plotted in Fig. 6. There are three distinct operating frequencies, with output power ~ 18 dBm to 20 dBm and total transmitter efficiency ~ 11% to 18% for each frequency. The total transmitter efficiency includes all sources of input power (including pad drivers and clock I/O). It should be noted that the efficiency is degraded due to a latch-up issue associated with the pads in the selected process that did not allow removal of the silicide block under the large pads. Latchup was verified due to a hysteretic current that could be reset by powering off the die and with a reference transmitter on the same die that demonstrated 7% higher PAE and 7dB higher output power [10], with no hysteresis. Latch-up is not an issue in processes that allow CUP structures, as the silicide block under the pads is not required.

The matching network is reconfigured for different center frequency of operation (e.g., 1.5 GHz, 1.7 GHz and 1.9 GHz) and different network quality factors by adjusting the values of the inductors $L_1$ and $L_2$. Capacitor $C_1$ (Fig. 4) is an on-chip capacitor that was used to help control the loaded quality factor of the matching network. $L_1$ and $L_2$ are wire-wound ceramic core inductors chosen for their high quality factor and favorable magnetic fields to limit losses in the substrate due to eddy currents. Passive component choices were made with parasitic aware SMD models, including effects for loading by the pads.

To validate the transmitter linearity, the amplifier’s performance is verified with a 5 MHz, 64 QAM LTE signal. A 2D, polynomial based DPD is applied to the MP-SCPA. The measured ACLR is plotted in Fig. 7 for two different operating
center frequencies, showing an ACLR < -30 dBc, while outputting an average power larger than 14 dBm. The signal constellation is also plotted in Fig. 8. The measured EVM is < 2.8%-rms. It should be noted that DPD is required primarily due to non-linearity associated with the bondwire inductance. Bondwire inductances cause the supply and ground to bounce when the circuit is switching. Using a flip-chip package and printed inductors can alleviate the requirements for DPD [16].

V. CONCLUSIONS AND FUTURE WORK
A package level technique that allows for easy reconfiguration of the RF matching network is demonstrated using an MP-SCPA in 130 nm CMOS. This packaging technique leverages the use of standard commercial wirebonds and SMD components to allow flexible alterations of the matching network to adjust for different power levels and output frequencies. The MP-SCPA is chosen as a reasonable first demonstration due to the fact that it presents a capacitive reactance to the matching network, allowing it to be easily matched using a pair of inductors. Though the technique was demonstrated for a transmitter, it is also valid for other chains in a transceiver (e.g., frequency generation and receivers). To validate the transmitter’s performance, it is measured using a 5 MHz, 64 QAM LTE signal at several different output frequencies. The ACLR and EVM are able to be controlled within their specifications. In future implementations, the size and latch-up can be controlled using CUP bondpads. Additionally, smaller SMD components are also available when using machine placement.

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