A SWITCHED-CAPACITOR POWER AMPLIFIER FOR EER/POLAR TRANSMITTERS

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Submission Highlight
A fully-integrated RF PA is presented that achieves EER/Polar operation via switched-capacitor techniques. It produces 25.2 (17.7) dBm of peak (average) output power with the highest average efficiency to date (32.1%) for a 20 MHz, 64-QAM OFDM modulated signal.

Abstract
A digitally-controlled switched-capacitor RF power amplifier is implemented in 90nm CMOS. It delivers a peak (average) output power of 25.2 (17.7) dBm with a peak (average) PAE of 55.2% (32.1%) for a 64 QAM OFDM modulated signal with a measured EVM of 2.9% in the 2.4 GHz ISM Band.

Text
Wireless high-speed communication standards such as WiFi, WiMax and LTE use spectrally-efficient OFDM modulation that encodes signal information in both amplitude and phase. Use of this non-constant envelope modulation requires a linear PA, operating at a less than peak signal level to realize higher linearity and inherently reduced efficiency. Because the PA is the dominant power consumer in most RF transceivers, operation with reduced efficiency leads to short battery lifetime and reduced mobility. Consequently, many efforts to utilize more efficient switching amplifiers with linearization circuitry have been made, notably through pulse-width modulation [1], outphasing [2] and envelope elimination and restoration (EER) [3],[4]. Of the three, EER offers the best performance tradeoff between linearity, output power and efficiency; however, most previous implementations have come at the cost of large, power-hungry analog supply modulators. Additionally, conventional EER techniques are subject to nonlinearity induced by delay mismatch between the amplitude- and phase-modulated signal components. An alternative solution modulated the output power by selecting multiple PA unit cells [5], but this exhibits low efficiency at low output power levels because the power control is achieved by changing the total PA transconductance through switching of inefficient unit class-A PA cells.

This paper introduces an EER power amplifier that achieves high output power, efficiency and linear output power control using a switched-capacitor based switching PA without the use of a supply modulator. To our knowledge, the 90 nm experimental prototype switched-capacitor power amplifier (SCPA) is the first of its kind. While amplifying 64-QAM OFDM modulation with a 20 MHz signal bandwidth it achieves an average output power of 17.7 dBm, an average PAE of 32.1%, and an EVM of 2.9%.
Switched-capacitor circuit techniques are widely used in analog/mixed-signal design because capacitors are area-efficient native devices and CMOS transistors are excellent switches [6]. High-accuracy capacitor ratios coupled with digital signal processing techniques are easily applied to switched-capacitor circuits. These techniques can now be adopted directly at RF frequencies because of the higher operating speeds associated with scaled CMOS. In a switched-capacitor circuit, any voltage can be generated based on the ratio of the capacitors switched to \( V_{DD} \) or ground \( (V_{GND}) \). It is important to note that there is no loss of energy ideally in the charge redistribution among capacitors (Fig. 1). To efficiently generate a desired output voltage, capacitors are selectively connected to either \( V_{GND} \) or switched between \( V_{GND} \) and \( V_{DD} \). Hence, the ratio of capacitors switching \((\Sigma C_{on})\) between \( V_{GND} \) and \( V_{DD} \) compared to the total capacitance \((\Sigma C_{on}+\Sigma C_{off})\) defines the output voltage. The capacitors are switched at the desired RF carrier frequency; a bandpass filter (BPF) (e.g., matching network) is created by connecting an inductive reactance in series with the capacitor array to select the RF signal to be broadcast by the SCPA. Because \( V_{DD} \) and \( V_{GND} \) are AC grounds, the total capacitance seen by the matching network remains constant regardless of the number of capacitors being switched; thus, the frequency response of the SCPA is constant and independent of the output voltage amplitude.

An SCPA operating as part of an EER transmitter is depicted in Fig. 2. A polar modulated signal is generated using baseband signal processing and the digital envelope signal \( (A) \) input to a thermometer decoder controls the number of unit capacitors to be switched, while the digital phase signal \( (\phi) \) synchronizes all switches selected by \( A \); i.e., delay mismatch is easily accounted for in DSP. The SCPA can be understood as capacitive power-combining of multiple individual switching PAs; i.e., the output power is combined via charge redistribution on the capacitors and then filtered by the bandpass matching network.

A single-ended implementation is shown in Fig. 3. The envelope code \( B_{en}(A) \) is processed in a binary-to-thermometer decoder which selects the capacitors to be switched while a dedicated buffer drives the switches connected to each capacitor. Digital logic gates subsequently synchronize and the envelope and phase information. To achieve higher output power, a supply voltage of \( 2V_{DD} \) is adopted by cascading the output switches. Inverter chains operating between ground and \( V_{DD} \) drive NMOS switches and inverters operating between \( V_{DD} \) and \( 2V_{DD} \) drive PMOS switches. A level shifter converts the PMOS drive signal from the nominal logic level to the higher supply voltage. To achieve high efficiency, a non-overlapping clock is used to prevent crowbar currents in the NMOS and PMOS switches, thus avoiding unnecessary power dissipation. The digital power consumption in the inverter buffer chains is proportional to the output voltage, due to fewer logic stages switching; hence, the roll-off in efficiency versus power backoff is less dramatic than in other PAs. Finally, the voltage generated by the switched capacitors is delivered to the BPF output matching network. The impedance presented to the capacitor array by the matching network is inductive; i.e., its reactance is used to negate the reactance of the capacitor array. The prototype SCPA is implemented differentially. Although the SCPA is designed for 6b resolution, more resolution can be
achieved with more unary/binary bits or using other switched-capacitor (e.g., C-2C ladder) or signal processing techniques (e.g., ΔΣ or pulse-width modulation).

The measured output power versus input code and PAE versus output power are shown in Fig. 4. The peak output power and PAE are 25.2 dBm and 55.2%, respectively, with a fully-integrated output matching network. As mentioned, the PAE has slower roll-off at power backoff than typical CMOS PAs; the PAE is 35.1% at power backoff of -6 dB from peak power. For comparison the efficiency characteristic of an ideal class-B PA scaled to have similar losses as the SCPA is also plotted. The linearity of the SCPA is characterized in Fig. 5; the measured output voltage and AM-PM distortion versus input code show weak second-order nonlinearities that are correctible by digital predistortion. The nonlinearity owes to the finite switch performance and power line impedance. Efficiency, output power and linearity are coupled in the design of the SCPA; optimum efficiency and output power are achieved with a reasonable tradeoff in linearity as demonstrated from dynamic measurements. A measured constellation for a 64-QAM OFDM modulated signal with a 20 MHz signal bandwidth is shown along with the measured output power spectral density (Fig. 5). A performance summary is given in Fig. 6.

A chip microphotograph of the 90 nm prototype is shown in Fig. 7. It is noted that both linearity and efficiency can be improved using a more advanced CMOS technology due to faster switching performance and lower digital power consumption in the driving buffers. Because the operation of the SCPA is based only on digital circuits such as logic gates, switches and capacitors, it is ideally suited for future scaled CMOS technologies.

References:


Captions:

Fig. 1: Switched-capacitor circuit for voltage modulation.
Fig. 2: Top-level implementation of an SCPA in a polar transmitter.
Fig. 3: Single-ended 6b SCPA; actual implementation is fully differential.
Fig. 4: Measured SCPA output power vs. input code and PAE vs. output power.
Fig. 5: (Clockwise from top left) Measured distortion vs. input code, frequency response, power spectral density and constellation for a 20 MHz 64-QAM OFDM signal.
Fig. 6: Performance summary.
Fig. 7: Chip microphotograph.
Fig. 1. Switched-capacitor circuit for voltage modulation.

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E_{in} = \frac{1}{2} \frac{C}{2} V_{DD}^2
\]

\[
E_{stored} = 2 \cdot \frac{C}{2} \left( \frac{V_{DD}}{2} \right)^2 = E_{in}
\]
Fig. 2. Top-level implementation of an SCPA in a polar transmitter.
Fig. 3. Single-ended 6b SCPA; actual implementation is fully differential.
Fig. 4. Measured SCPA output power vs. input code and PAE vs. output power.
Fig. 5. (Clockwise from top left) Measured distortion vs. input code, frequency response, power spectral density and constellation for a 20 MHz 64-QAM OFDM signal.
<table>
<thead>
<tr>
<th>Technology</th>
<th>90nm CMOS</th>
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<tbody>
<tr>
<td>Resolution</td>
<td>6 bits</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.25V / 2.5V</td>
</tr>
<tr>
<td>Output Power (Peak/64 QAM OFDM)</td>
<td>25dBm / 17.7dBm</td>
</tr>
<tr>
<td>PAE (Peak/64 QAM OFDM)</td>
<td>52.9% / 32.1%</td>
</tr>
<tr>
<td>EVM (64 QAM OFDM)</td>
<td>2.9%</td>
</tr>
<tr>
<td>Frequency</td>
<td>1.8GHz – 2.8GHz</td>
</tr>
<tr>
<td>Die Area</td>
<td>1.04mm$^2$</td>
</tr>
<tr>
<td></td>
<td>(0.73mm$\times$1.43mm)</td>
</tr>
</tbody>
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Fig. 6. Performance Summary.
Fig. 7. Chip microphotograph.