A Quadrature Switched Capacitor Power Amplifier in 65nm CMOS

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Abstract—This paper presents a quadrature switched-capacitor power amplifier (SCPA) that achieves similar output power and efficiency as polar/EER based digital PAs. It combines in-phase (I) and quadrature (Q) signals on a shared capacitor array in the charge domain. The SCPA utilizes a class-G dual-supply architecture to improve efficiency at backoff. This counteracts losses associated with the signal combination. Unlike polar/EER counterparts, the quadrature SCPA requires no wideband phase modulator or delay matching circuitry. The SCPA delivers a peak output power of 20.5 dBm with a peak PAE of 20%.

Index Terms—Class-D PA, Digital PA, EER, Quadrature PA, Polar PA, Switched-Capacitor PA, SCPA.

I. INTRODUCTION

The RF power amplifier continues to be the largest obstacle to complete integration of RF systems-on-chip. This owes to the low voltages allowed for safe operation of fine line CMOS transistors, coupled with lossy passive components (e.g., spiral inductors and transformers) and poor functionality as a transconductor. CMOS scaling has made the device a lower loss, faster switch; hence to leverage the benefits of scaling, amplifier topologies that use the transistor as a switch should be favoured.

Switching amplifiers have shown to be more efficient than their linear amplifier counterparts and several techniques have been optimized recently to linearize their operation, including envelope elimination and restoration (EER) [1], digital PAs [2]–[4], Doherty [5], and outphasing [6]. Of these topologies, the digital PA topologies offer the highest degree of flexibility, as the signal is input to the PA as a digital code word and the PA acts as a digital-to-analog converter in the amplitude domain, a frequency upconverter and amplifier all-in-one [2]–[5].

The aforementioned Polar techniques translate a signal from Cartesian coordinates (e.g., I(t), Q(t)) to polar coordinates (e.g., A(t), φ(t)), using the following transformations:

\[ A(t) = \sqrt{I^2(t) + Q^2(t)} \]
\[ \phi(t) = \tan^{-1}(Q(t)/I(t)) \]

Owing to the strong non-linearity associated with these conversions, the bandwidth required for the amplitude paths and phase paths is substantially larger than the bandwidth of the Cartesian components.

Shown in Fig. 1 is an alternative to polar domain PAs is to leverage the improved efficiency of digital amplitude modulation in the Cartesian domain to amplify the I and Q signals independently and combine in the charge domain on the capacitor array. In this way, amplitude and phase modulation can be achieved by weighting the I(t) and Q(t) vectors appropriately, relative to one another. All four quadrants can be output simply by inverting the phases of the I(t) and Q(t) vectors, respectively. Similar techniques have used a transformer for this combination; however due to interaction of currents in the transformers winding, this technique requires significant predistortion [7].

Because of the phase difference between the two vectors, the maximum output amplitude after combination is 70.7% of the peak amplitude of either vector. The class-G SCPA operates at high efficiency, by appropriate scaling of the supply voltage and disabling output cells when not required [3]. In this paper we present a capacitor combined class-G SCPA for non-constant envelope amplification. Though the efficiency of this PA is lower than traditional polar/EER based DPAs, but this PA does not require a wide-band or
an open loop phase modulator [8]. Because the I and Q signals propagate with similar frequency and bandwidth, timing alignment is also not as critical as in a polar/EER based DPA; hence no synchronization between signal paths is necessary.

This paper is organized as follows. In section II, design details of the transformer combined quadrature SCPA are presented. This section is followed by measurement results in Section III. Finally, conclusions and future work are presented in Section IV.

II. THEORY OF OPERATION FOR A CAPACITIVELY COMBINED QUADRATURE SCPA

Switched-capacitor circuits are ubiquitous in CMOS owing to the ability to create low-loss switching circuits and to precisely control the ratio of different capacitors on the same integrated circuit. The switched-capacitor PA is essentially a class-D power amplifier with a controllable output charge division; hence a controllable output voltage amplitude. A detailed description of the theory of operation of a class-G SCPA can be found in Yoo, et. al. [3].

The proposed quadrature SCPA is shown in Fig. 1. In the proposed architecture, the digitized in-phase and quadrature signals, \( B[I(n)] \) and \( B[Q(n)] \), are input and decoded into unary and binary codes. These bits are buffered to drive the bottom plates of an arrayed capacitor with a shared top plate. Using a class-G SCPA allows for higher efficiency at output power backoff because the amplifier can operate from a lower supply voltage during periods in the signal where the output envelope is small. [3].

The bottom plates of the respective I and Q sub-arrays are clocked by a quadrature clock. An on-chip divide-by-two circuit generates the quadrature clock signals. The charge on the array is a vector summation of the I and Q signals given by the following:

\[
I(t) = A_I(t) \cdot \cos(2\pi f_{RF} t) \\
Q(t) = A_Q(t) \cdot \sin(2\pi f_{RF} t).
\]

\( A_I(t) \) and \( A_Q(t) \) represent the weighting of the I and Q signals, respectively.

Care must be taken to ensure symmetric loading in the I and Q paths to maintain similar signal delay. It should be noted that this matching is less critical than that of a Polar/EER PA, because the I and Q signals propagate at the same frequency, whereas envelope and phase signals in polar PAs propagate at significantly different frequencies.

The amplitude, \( A(t) \) of the combined I(t) and Q(t) signals given is by the following:

\[
A(t) = \sqrt{A_I^2(t) + A_Q^2(t) \cdot \sin(2\pi f_{RF} t + \tan^{-1}\left(\frac{A_Q(t)}{A_I(t)}\right))} \tag{5}
\]

This function is maximum when \( A(t) = A_I(t) \) and can be reduced to the following:

\[
A_{\text{max}}(t) = \sqrt{2} \cdot A_I(t). \tag{6}
\]

The maximum if the clocking signals were in phase would be \( 2A_I(t) \); The ratio of these two maxima represents the system efficiency, \( \eta_{\text{quadrature}} \), of the quadrature combining scheme:

\[
\eta_{\text{quadrature}} = \frac{\sqrt{2}}{2}. \tag{7}
\]

As previously mentioned this system does not suffer the same non-linearities associated with polar/EER PAs.

A. Design of the unit class-G SCPA

A block diagram of the unit class-G SCPA is shown in Fig. 1; a single-ended version is shown although the fabricated circuit is fully differential. First, a Cartesian representation of a non-constant envelope signal is separated into its constituent in-phase, I, and quadrature, Q, vectors. The digitized I and Q vectors, \( B_{\text{in}}(I,Q) \), are represented as signed digital code words; These vectors are input to a digital pattern generator that separates the bit pattern and outputs the bits to their proper digital inputs. The MSB is the sign bit and is input to an LVDS clock receiver wherein the output phase of the LVDS circuit can be inverted (non-inverted) if the sign bit is high (low).

The remaining bits represent the amplitude weighting of the I and Q signals. Each capacitor array comprises a total of 6 bits. This resolution is chosen to reduce the quantization noise at the output of the system to acceptable levels, while allowing for potential digital predistortion (DPD).

The capacitor array is sub-divided into a unary array and a binary array as a compromise between size/complexity and linearity. The four MSBs are unary-weighted and controlled by a binary-to-thermometer decoder whereas the two LSBs are binary-weighted for fine output resolution. An extra bit is achieved by operating with two different
In order to minimize the losses resulting from large impedance transformation ratios, it is desirable to operate from larger voltage supplies. This is accommodated by cascading the CMOS inverter that acts as the switch between the high supply voltage and ground. Using this arrangement and setting the gate voltage on the cascade transistors (MN2 and MP2) to VDD allows the supply voltage to be raised to twice VDD, which is labelled VDD2. This stacking also ensures that no terminal-terminal voltage ever exceeds VDD.

In order to accommodate class-G operation, a second switching path is added that operates from a lower supply voltage. In this design, VDD is used so that an extra bit of resolution can be achieved owing to the binary scaling of the supplies. Transistors MN3 and MP3 are added to switch to this supply when the envelope amplitude is smaller than VDD. In this off-state (e.g., \( A(t) > V_{DD} \)), the gates of MN3 and MP3 are set to \( V_{DD} \), both switches remain off while the output node swings as high as VDD2. In the on-state (e.g., \( A(t) < V_{DD} \)), MN3 is set to \( V_{DD2} \) and MP3 is switched between VDD and VGND. Care must be taken to ensure that the switching resistances in the VDD2, VDD and VGND paths are well matched. If they are not matched there will be code-dependent non-linearity leading to AM-AM and AM-PM distortion that will require DPD to resolve.

The capacitor array is designed using MiM capacitors and all of the top-plates are connected together, while the bottom plates are connected to switches. The top plates are connected in series with an inductor, \( L_{ser} \), forming a bandpass series-resonant circuit at the design frequency. Because the total capacitance remains unchanged from the perspective of the inductor, the inductance can be sized to be series resonant with the total capacitance in the array. This circuit acts to filter the undesired harmonic content associated with switching.

The inductor \( L_{ser} \) is realized as part of an impedance transformation circuit, wherein \( L_{ser} \) is a positive residual reactance looking towards the load resistance (e.g., 50 \( \Omega \)). The impedance transformation circuit uses a loaded quality factor, \( Q_{loaded} = 5 \), leading to a circuit with approximately 400 MHz 3-dB bandwidth centered at 2 GHz. Higher quality factors can be used if off chip impedance transformation is used owing to the higher quality factor of off-chip components.

III. MEASUREMENT RESULTS

An experimental prototype of the transformer combined quadrature class-G SCPA is fabricated in a 65 nm RF CMOS process with an ultra-thick top metal for high quality passive elements. A chip microphotograph of the SCPA is shown in Fig. 3. The PA operates at a center frequency of 2 GHz with a peak output power and efficiency of 20 dBm and 21%, respectively, as shown in Fig. 4. The -3 dB bandwidth of the PA is \( \approx 400 \) MHz as determined by the loaded quality factor of the band-pass matching network. Note that the performance below 2 GHz is dominated by the rolloff of the balun in the measurement setup. To verify the function over the code range of quadrature inputs, the output power and PAE are plotted for the vector \( I=Q \) in Fig. 5. The output amplitude and PAE reduce linearly as the code is changed. A sign bit allows the quadrature oscillator signals to be inverted so that all quadrants of the complex plane are accessible. Asymmetry in the response owes to supply and ground bounce due to excess bondwire inductance in the PCB layout. This has been reduced in a subsequent layout and will result in higher symmetry and linearity, as verified by simulation. To demonstrate the performance along a constant phase output a fixed 45 phase is input to the PA, where \( I=Q \). To verify the quadrature SCPAs ability to amplify complex modulated signals, a 5 MHz, 64 QAM LTE signal is applied to the power amplifier. The ACLR performance is plotted in Fig. 6 and shows less than -30 dBc when outputting 14.2 dBm at 12% average efficiency. This result is obtained after a 2D digital pre-distortion procedure that is only necessary due to the aforementioned excessive supply and ground bondwire inductance. The measured EVM at this ACLR is 4%-rms. The signal constellation is plotted in Fig. 7. The functionality of the QSCPA is validated through both the static and vector measurements. The advantages of the
QSCPA are evident in that no phase modulator or timing synchronization circuitry was necessary.

IV. CONCLUSIONS AND FUTURE WORK

A quadrature SCPA that can output any phase and amplitude on the complex plane based on digitally coded quadrature inputs is demonstrated in 65nm CMOS. This PA leverages the advantages of digital PAs while not requiring the wideband modulator of typical PAs. The performance of the PA is validated using static measurements and measured with a 5MHz, 64-QAM LTE signal. After a 2D DPD, the ACLR is below the required -30 dBc limit and the measured EVM is <4%.

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