Digital Power Amplifier: A New Way to
Exploit the Switched-Capacitor Circuit

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Abstract—A digital power amplifier (DPA) that uses switched-capacitor circuits in 90 nm CMOS to efficiently amplify signals with large peak-to-average power ratios is described in this article. In traditional DPAs, a digital code word representing a desired output envelope voltage is used to control a combination of wide-dynamic range current sources. In contrast, the Switched-Capacitor Power Amplifier (SCPA) provides a linear output characteristic by using the digital code word to selectively switch or not switch a bank of integrated capacitors at the RF carrier frequency. Therefore, the SCPA combines the functionalities of an envelope DAC and a power amplifier, and achieves excellent efficiency and output power levels. The SCPA benefits from CMOS transistor scaling which makes RF SOC integration realizable.

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The demand for increasing data-rates over the wireless channel coupled with the high cost of available spectrum has led to the greater use of spectrally-efficient modulation techniques wherein information is stored in both the instantaneous phase and amplitude of the signal. Such non-constant envelope (non-CE) modulation places additional burdens on all elements of the wireless transceiver, as typically more power is required to ensure low noise performance to guarantee adequate signal-to-noise (SNR) for demodulation. Non-CE modulation places the severest demands on the RF power amplifier (PA) where amplification of a non-CE modulated signal requires that the PA operate at low-efficiency power backoff level.

The RF PA is designed to achieve its peak efficiency while operating at its peak, or saturated output power level. Non-CE modulated signals with large peak-to-average power ratios (PAPR) (e.g., orthogonal frequency division multiplexing (OFDM), quadrature amplitude modulation (QAM), etc.) dictate that the amplifier will, on average, not be operating near the highest-efficiency region of operation and, hence, will offer low average efficiency. This is exacerbated in CMOS where traditional linear PA architectures which use transistors operating as linear transconductors operate with low peak efficiency because of voltage stress limitations and relatively low power gain, as compared to RF PAs constructed using compound semiconductor materials.

CMOS transistors have been scaled at an aggressive rate for more than fifty years, reducing the transistors minimum feature size (e.g., transistor gate length) by a $\sqrt{2}$ factor every two years. This has led to faster switching transistors at the expense of lower operating voltages due to the reduced transistor breakdown limits that scale proportionally with the device size. Scaling also has had a deleterious effect on the transconductance and output resistance, eventually limiting
the linearity of scaled CMOS amplifiers. As a result, the so-called “switch-mode” PA has been investigated heavily in recent years. Switch-mode PAs (e.g., class-D, -E, and -F, etc.) are more efficient than linear PAs due to waveform shaping that reduces power dissipation in the transistor at the expense of sensitivity to the amplitude of the input waveform. This means that external linearization circuitry is needed in these topologies, which has hindered incorporation of the PA into RF systems-on-a-chip (SOC).

A digital power amplifier (DPA) incorporates the functionality of a digital-to-analog converter and power amplifier into the same circuit and can be used in combination with polar transmitter architectures (e.g., envelope elimination and restoration) to leverage switched-mode PA efficiency advantages while linearly amplifying non-CE modulated signals.

**DIGITAL POWER AMPLIFIER REVIEW**

The previous research on DPAs, which motivated the switched-capacitor PA (SCPA) concept, is described in the following sections. The two dominant types of DPAs are pulse-width modulated (PWM) and digitally-controlled current/voltage signal summation amplifiers.

**PWM DPA Architectures**

In the basic PWM DPA architecture, a Cartesian representation of a signal is transformed to its polar equivalent where the amplitude-modulated component is encoded as the duty cycle of a pulse and the phase-modulated portion is encoded in the position of the leading edge, as shown in the top portion of Fig. 1. By changing the duration/width of the pulse, the energy input to the filtering network is varied. Hence, if a bandpass filter is used to select the energy at the desired frequency, a waveform with amplitude proportional to the duration of the input pulse and an instantaneous phase proportional to the phase of the leading edge is output from the PA. A conceptual block diagram for such a PWM DPA is shown in the bottom half of Fig. 1. It is
comprised of a digital PWM modulator driving a switched-mode power amplifier that uses a bandpass matching network.

If the average time between pulses is proportional to the inverse of the desired RF carrier waveform, the modulation method is known as bandpass PWM and no additional RF signal up-conversion in frequency is necessary; hence, the modulation can be generated entirely in a fast digital signal processor [1][2]. Additionally, this type of waveform is “digital” in nature because the absolute amplitude of the input switching waveform is not transferred to the output so long as it is large enough to turn the switching transistor on with a sufficiently small switching resistance.

The switched-mode RF PA can be chosen as any of the common switching amplifier topologies [3][4][5][6]; however, the class-E topology has shown significant promise in CMOS implementations because it more optimally absorbs the parasitic capacitance of the driver transistor into the output wave-shaping network [7].

The main drawback with PWM topologies is that because the average pulse width is inversely proportional to the RF carrier frequency, the minimum pulse duration that can be processed without pulse-swallowing sets the dynamic range. Ultimately, these types of amplifiers are limited to signals with PAPR ≈ 6-10 dB at the frequencies commonly used for high-speed wireless communication (e.g., 2.4 and 5.6 GHz) [7].

*Summing DPA Architectures*

The summing DPA of Fig. 2 adds the RF currents or voltages of a large number of unit cells operating as amplifiers/gain stages [3][8][9]. In the DPA, a unit amplifier is designed to operate as a linear transconductor (e.g., a voltage-dependent current source) whose biasing can be selectively activated. A digital amplitude word controls amplitude selection logic that
enables/disables selected unit cells. These unit cells can operate as linear transconductors for small input amplitudes, or as saturated current sources for large input amplitudes. The basic operating assumption is that a unit cell operating near its saturated output is more efficient than a conventional linear amplifier operating at reduced output power, because the quiescent current required to bias a transistor is dissipated regardless of the size of the envelope voltage. The efficiency of the summing DPA typically is proportional to the square root of the output voltage amplitude.

The operation of the DPA is most efficient when operating on polar signals where the Cartesian representation of a signal is transformed to its equivalent polar representation, which can be done in digital signal processing using a CORDIC algorithm. The amplitude modulated (AM) and phase modulated (PM) signals can then be routed to the amplifier in two different paths. The PM signal, modulated at the RF carrier frequency, is routed to the traditional input to the unit cell amplifier (e.g., the gate of a CMOS common-source stage); meanwhile, the AM signal is encoded as an amplitude code word and applied to the selection logic to control the biasing of a selected number of unit amplifier cells. Thus, power is saved because unit cells that are not contributing to the output are disabled.

The drawback of such an approach is that the desired characteristic for a transconductor is large output impedance for linear operation as a current source. CMOS transistors in scaled processes have ever decreasing output conductance and, as such, do not behave like linear current sources unless techniques such as cascoding are applied. Cascoding increases the voltage headroom required for operation as a current source. In either case, the output voltage characteristic of the amplifier saturates and becomes nonlinear as the input code word becomes large. This effect can be overcome using digital calibration techniques, but such techniques
require extra bits of resolution to achieve a desired linear response and increase power consumption and die area. Nonetheless, the digital RF processor proposed in [10] successfully implemented such a DPA.

**The Proposed SCPA Architecture**

The power amplifier must be designed to linearly amplify a non-CE signal with a high average output power and high average efficiency, while adding minimal distortion to the signal. Most of the aforementioned digital PA techniques utilize the PA as a linear transconductor; that is, the unit amplifier cell converts the input voltage signal to a current that is linearly proportional to the voltage applied to the input. Deeply-scaled CMOS transistors are poor linear transconductors. Thus, their linearity performance is poor and must be compensated using calibration techniques or predistortion of the input signal, which ultimately require extra bits of resolution or additional power to provide the required linearity [11]. Moreover, calibration to correct severe nonlinearity could require a complex system to compensate including standard process, voltage, and temperature (PVT) variations.

The SCPA technique differs from the aforementioned DPA techniques in that it utilizes the CMOS transistor in its optimal roll as a switch and achieves high accuracy/linearity by exploiting the precision of capacitance ratios that CMOS processes provide (Fig. 3). Because the linearity of the SCPA is not dependent on the linearity of the transistor, careful switch design and layout techniques can eliminate the need for calibration/predistortion circuitry in moderate resolution designs and reduce the complexity in higher resolution designs. The elimination, or reduction, of predistortion results in an associated reduction in the chip area and power consumption.

Switched-capacitor circuits are ubiquitous in CMOS because they utilize only the native elements available in all CMOS processes; namely, transistors and precision capacitors [12][13].
Conceptually, an SCPA (Fig. 3) is designed as an array of capacitors that can be either switched between two different voltage potentials (e.g., $V_{\text{gnd}}$ and $V_{\text{DD}}$) or held at a fixed voltage potential (e.g., $V_{\text{gnd}}$ or $V_{\text{DD}}$). The capacitor array is designed such that all of the capacitors share a common top plate, while the bottom plate of each capacitor is controlled by a switch. The common top plate of the capacitor array is then presented with a bandpass matching network that serves two purposes. First, the switching operation generates significant harmonic components from a square wave; the bandpass matching network selects the fundamental component of the switching waveform and attenuates all harmonics. Second, the bandpass network transforms the impedance presented by the antenna (e.g., 50 $\Omega$) to a lower impedance (e.g., 4 $\Omega$) so that high output power can be generated.

The voltage level of the SCPA is controlled via charge sharing between the capacitors that are switched ($\sum C_{\text{ON}}$) and the capacitors that are held at fixed potential ($\sum C_{\text{OFF}}$). Thus, the output voltage at the top-plate of the capacitor array is given as:

$$V_{\text{out}} = \frac{\sum C_{\text{ON}}}{\sum C_{\text{ON}} + \sum C_{\text{OFF}}} \cdot V_{\text{DD}}$$ (1)

An example of this can be discerned from Fig. 3. Examining the left half of the figure, all capacitors $C_0$-$C_7$ are switched between $V_{\text{gnd}}$ and $V_{\text{DD}}$; hence, $\sum C_{\text{ON}} = \sum_{i=0}^{7} C_i$ and $\sum C_{\text{OFF}} = 0$ and the output voltage swing is equal to $V_{\text{DD}}$. In the right half of the figure, only half of the capacitors are switched; hence, $\sum C_{\text{ON}} = \sum_{i=0}^{3} C_i$ and $\sum C_{\text{OFF}} = \sum_{i=4}^{7} C_i$ and the output voltage swing is equal to $V_{\text{DD}}/2$.

The SCPA is designed by dividing the capacitor array into multiple bit slices, where the number of bit slices corresponds to the resolution required for amplification of a desired non-CE signal (Fig. 4) [11][14]. The top plate of each capacitor is shared, and hence a charge domain summation of each bit slice is performed before the output of the capacitor array is fed into a
bandpass filtering/matching network. The designs of two key circuit blocks are discussed in the following sections; namely, the low-loss switches to deliver high output power and the passive bandpass matching network.

**Switch Design for SCPA**

The switch design for the SCPA is shown in Fig. 5. One of the greatest challenges in designing CMOS PAs is that the breakdown voltage of CMOS transistors is limited due mainly to the strong electrical fields concentrated in the thin gate oxides. The output power, $P_{out}$, in a power amplifier is proportional to the supply voltage:

$$P_{out} \propto \frac{V_{DD}^2}{R_{out}} \quad (2)$$

where $R_{out}$ is the optimal termination resistance. Because of the limited voltage supply available in a scaled CMOS process, a small output resistance is required, which leads to low gain. A lower output impedance is created using a passive matching network that transforms the antenna impedance from a typical value of 50 $\Omega$ to a value dependent on the desired output power. The loss in the matching network is proportional to the impedance transformation ratio (ITR) due to loss in the passive matching components (e.g., inductors and capacitors). In order to achieve high output power a large ITR is necessary, resulting in significant power and efficiency losses. To alleviate this loss it is beneficial to operate from a larger supply voltage; hence, the switch design utilizes cascoded NMOS and PMOS switches where the NMOS transistors are switched between $V_{gnd}$ and $V_{DD}$ and the PMOS devices are switched between $V_{DD}$ and $2V_{DD}$ [15]. Additional cascode transistors could be employed to raise the allowable supply voltage above $2V_{DD}$ at the expense of additional loss in the switch; hence, an optimization exists between loss in the output matching network and in the switch. In the presented SCPA, a single cascode resulted in
optimum output power and efficiency; however, this tradeoff should be examined carefully for the devices available in the given CMOS process development kit.

**Passive Filter/Matching Network**

The passive matching network must accomplish two main goals: 1) It should provide filtering of the high-order switching harmonics associated with driving the switching transistors, and 2) it must present a lower impedance to the capacitor array so that high output power can be achieved. Because the impedance looking towards the array is dominated by the capacitance of the array, the matching network must be designed to be resonant with the total capacitance of the array.

In practical RF circuits, the selectivity of the filtering available from a network is limited by the quality factor ($Q$) of the passive components that comprise the filter. In the case of CMOS processes, the quality factor of the inductor (~10-15) dominates that of the capacitor; furthermore, the quality factor of the network, $Q_{\text{loaded}}$, should be approximately 5 times lower than any individual component of the network. This limits $Q_{\text{loaded}}$ to practical values of 2-3.

In the SCPA, output power and voltage levels are used to determine $R_{\text{opt}}$ and coupled with $Q_{\text{loaded}}$ to determine the optimum value for the total array capacitance; hence, the only remaining design option is the network topology of the matching network. Though the network will have a bandpass characteristic in general because of the desire for a low impedance path toward the antenna (e.g., series resonance), a topology that utilizes inductors in series with the output is desirable because of the additional attenuation that series inductors provide to high frequency signals.
**SYSTEM SPECIFICATIONS**

The SCPA is designed to output 24 dBm with 6-b resolution in the amplitude domain allowing it to work well over the envelope voltages typical for WiFi communication standards. The resolution is designed to be widely tunable over any resolution less than its peak amplitude by changing the digital code word that is input to the decoder. Demonstration of the system is proven by amplifying an IEEE 802.11g signal that has a signal bandwidth of 20 MHz, with a 64 QAM OFDM modulated signal with PAPR = 13 dB.

*Bit Slice Design Strategy*

Each element in the capacitor array is designed as a 1-bit slice and the associated switch driver and logic circuits that comprise the slice are pitch-matched to the width of the bottom plate of the capacitor. In this manner application specific designs can be made by increasing/decreasing the number of slices in the array and changing the length of the capacitor to adjust for the desired $Q_{loaded}$. This strategy enables use of traditional DAC design strategies to minimize layout specific errors by employing techniques such as dynamic element matching. Frequency tuning of the PA can be achieved using a tri-state switch to allow part of the capacitor array to float, effectively changing the total capacitance in the array and hence the center frequency of the resonance.

*DAC Resolution*

The resolution of the array can be controlled by properly selecting the number of bit slices employed in the design. The WiFi application chosen to verify the performance of the SCPA requires an error vector magnitude (EVM) < 5.6% to demodulate the signal, and must meet the spectral mask dictated by the FCC. System simulations were performed to verify that 6-b resolution was sufficient to amplify the WiFi signal with sufficient margin to both the EVM and
spectral standards as dictated by the large PAPR (≈13 dB) of the WiFi signal. Nevertheless, owing to the bit slice design strategy an additional 1-2 bits can be added to the array without necessitating too much stress in layout matching, which could allow the SCPA to be scaled to WiMAX applications.

**Linearity**

Linearity in the PA is dictated by the conversion of the envelope modulated signal into additional AM modulation (AM-AM) and phase modulation (AM-PM) through various non-linearities; however, it should be noted that AM-PM distortion is more problematic than AM-AM distortion in the SCPA because of the superior matching achievable in CMOS technologies. The main contribution to AM-PM distortion follows from the fact that the actual impedance is changing depending on the code because transistors are not ideal switches; parasitic resistances and capacitances in NMOS and PMOS transistors are different and physical operation of the MOS transistor requires time to turn on and off. It is exacerbated with the use of cascoded switches and the non-overlapping NMOS and PMOS operation used to achieve higher output power and efficiency. These results create dynamic, amplitude-dependent time constants that manifest themselves as instantaneous changes in the timing of the signal (e.g., phase modulation). Care in designing the NMOS and PMOS switches for matching alleviates much of this AM-PM distortion. It should also be noted that as CMOS transistors scale, the switching performance improves and thus both AM-AM and AM-PM distortion improve [11].

**MEASUREMENT RESULTS**

The SCPA is implemented in a 90nm CMOS process with a die area of 730×1430μm² (Fig. 6). Die area is dominated by the matching network. Note that the active circuit area is only ~25%
of the total area; hence, extra resolution in the DAC will incur minimal penalty in the overall implementation area. The SCPA achieves a peak (average) output power of 25.2 (17.7) dBm and a peak (average) efficiency of 45 (27) % while amplifying an IEEE 802.11g signal.

The dynamic performance of the SCPA is verified by measuring an IEEE 802.11g signal with digital predistortion determined from the static measurements. Excellent EVM performance of 2.6%-rms was demonstrated, which is well below the specification. The measured power spectral density (PSD) violates the FCC mandated spectral mask for two main reasons. The close in spectral mask violation is consistent with a time-synchronization mismatch in the AM and PM signal paths, mainly due to difficulty in synchronizing off-chip signal generators [16]. Simulation results show excellent signal path matching on chip and excellent spectral performance. The far out spectral mask is violated due to upconversion of the AM sample clock to RF frequencies, an effect that can be lessened by operating the sample clock at higher frequencies, or using signal processing techniques such as dithering of the clock signal to whiten it to lower the noise floor of the PA.

Additional improvements to output power can be achieved using power-combining techniques to make the SCPA adequate for cellular and other wide area network applications [17].

REFERENCES


FIGURE CAPTIONS

Fig. 1. (Top) Example of pulse-width and location modulation and (Bottom) Conceptual block diagram of a PWM DPA, comprising a PWM modulator, switching RF PA and filtering/matching network.

Fig. 2. Summing digital PA (DPA) unit cell and block diagram.

Fig. 3. SCPA conceptual operation (left) all capacitors (C₀-C₇) switching between $V_{DD}$ and $V_{gnd}$ outputs maximum power (right) half total capacitors (C₀-C₃) switching between $V_{DD}$ and $V_{gnd}$ and half total capacitors (C₄-C₇) held at $V_{gnd}$ outputs half power.

Fig. 4. Block level SCPA architecture

Fig. 5. SCPA switch and driver schematic

Fig. 6. SCPA Results (clockwise from upper left): Chip-microphotograph, spectral performance, static power and efficiency characteristics and vector signal performance (IEEE 802.11g).
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