A 28.6dBm, 65nm Class-E PA with Envelope Restoration by Pulse-Width and Pulse-Position Modulation

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Abstract

A class-E PA with on-chip pulse-width and pulse-position modulator (PWPM) for envelope restoration is fabricated in a 65nm process. It operates from a 2.5V supply and the die area is 1.3x1.6mm. It achieves a measured $P_{out}$ of 28.6dBm with a PAE of 28.5%. It can amplify phase-modulated signals and signals of limited peak-to-min ratios. It achieves EVM values of 1.2%-rms and 4.6%-rms for a GMSK signal with symbol rate of 270kHz and a $\pi/4$-DQPSK signal with symbol rate of 192kHz, respectively.

The desire for near-watt level output power in nanometer CMOS is difficult to satisfy owing to the power supply voltage scaling with minimum feature size. High-performance is problematic because most PA interfaces are defined by a 50$\Omega$ characteristic impedance whereas the optimum termination for a near-watt level output is $\sim$1-5$\Omega$. A large output power is usually obtained using either a passive matching network, or a power combiner with multiple PAs [1]. A significant loss is incurred in either network. Switching amplifiers exploit the ever improving switching performance of CMOS transistors to provide high power output and the simplicity of the output network to attain good power efficiency. However, because switching PAs are non-linear with respect to input amplitude, they cannot, under normal driving conditions, amplify a modulated signal with a non-constant envelope (CE). Complicated systems employ supply modulation to restore the signal envelope [1]. But, the overhead circuitry required for systems with large envelope variations is not necessarily required for systems with moderate envelopes. To the authors’ knowledge, this paper introduces the first class-E PA that overcomes these limitations using pulse-width and pulse-position modulation (PWPM).

The output amplitude of a class-E PA is somewhat sensitive to variations in the duty cycle of the input signal, a feature that is effectively combined with PWPM to amplify non-CE signals without using a supply modulator (Fig. 1). In a class-E switching power amplifier, the supply inductor integrates the current that flows from the supply through the switch when it is closed. When it is opened, the stored energy is transferred through a series resonant network to the output. Maximum power output is obtained for an input signal with a 50% duty cycle.
As the duty cycle is reduced, the energy stored in the output network is also reduced; i.e., the output power is controllable via the input duty cycle variations. The power transfer characteristic versus input signal duty cycle is non-linear, a fact which can be explained by taking the Fourier transform of a pulse train and observing the amplitude of the fundamental as duty-cycle is varied. Additionally, circuit non-idealities further contribute to the nonlinearity of the $P_{\text{out}}$-duty cycle characteristic. Nevertheless, this nonlinearity is easy to eliminate using a digital pre-distortion technique. The dynamic range of the PA is limited by the minimum pulse width that can be processed through the driver and PA without being swallowed; thus, the PWPM technique described herein is applicable for signals with moderate peak-to-minimum ratios.

Class-E amplifiers exhibit significant voltage swings that might overstress the switching device [2]. As a result, most previous class-E amplifiers cannot operate at the rated maximum supply voltage of the process, which exacerbates the impedance matching conditions. A class-E amplifier with a finite DC feed inductance reduces the stress applied to the switching device [3]. Moreover, in most modern CMOS processes, thick-gate I/O devices are available for use in chip I/O interfaces. Hence, voltage stress on the switching devices is further reduced using a thick-gate device connected in cascode with the switch device. As a result, the maximum voltage swing for all devices never exceeds the rated maximum supply voltage of any device by more than 1.8X [2]. The resulting class-E PA is shown in Fig 2. It is designed so that the outputs of four smaller pseudo-differential pairs are summed at the output under the control of bits $b[0-3]$. This approach reduces thermal stress on the devices without significantly increasing the source inductance. Additionally, coarse power control is achieved by setting the digital states of the bit lines that enable the driver; i.e., power control is realized by increasing the effective resistance of the output stage switch.

The output network consists of the shunt capacitance from the cascode device, along with the slab inductor, which acts as both the DC feed and a tuning element to counteract excess capacitance from the device. Due to the lack of an ultra thick metal (UTM), the slab inductor comprises the top two metal layers connected with vias and is designed to handle the large average current the PA requires. The matching network and series resonant
filter necessary for the class-E operation are implemented using a spiral inductor and a tapped-C network consisting of two MOM capacitors.

In order to characterize the PA versus duty cycle, a PWPM generator is realized on chip (Fig. 2). It consists of a clock receiver and re-timer followed by a NOR gate that generates a pulse when the outputs of both clock receivers are low. Two generators apply signals to the two clock receivers and the phase of one signal generator is swept relative to the other to generate different pulse widths. The PA is driven using a broadband digital inverter chain with a small taper factor in order to accommodate narrow pulses. This is at the expense of increased power in the driver chain and a subsequent reduced PAE. The PA operates from two different supply voltages—the drivers from 1.5V and the output stage from 2.5 V. The measured output power and power added efficiency of the PA are shown in Fig. 3. It achieves a peak output power of 28.6 dBm with a PAE of 28.5%. Power control using the bit lines is illustrated in Fig. 3; specifically, with only one bit enabled the output power is reduced to 21 dBm with a PAE of 13%. PA performance versus frequency is shown in Fig. 4. The 3-dB bandwidth is 900 MHz with a center frequency of 2.2 GHz.

To demonstrate the fidelity of the PA to a modulated signal, it is tested with a CE GMSK-modulated signal with a symbol rate of 270 kHz. The measured output for such a signal is shown in Fig. 5. With 27.5 dBm output power, the PA achieves a measured EVM of 1.2%-rms. Fine power control over a 6 dB range is achieved by adjusting the relative phase of the input signals and coarse power control is achieved by using the bit lines. The PA characteristics were also measured using a non-CE $\pi/4$-DQPSK modulated signal with a symbol rate of 192 kHz. Because the output envelope amplitude is not linear with duty cycle, a calibration procedure is used to pre-distort the input signal. The measured output for such a signal is shown in Fig. 6. With 26.7 dBm output power, the PA achieves a measured EVM of 4.6%-rms.

A chip microphotograph of a prototype class-E PA for PWPM modulation that achieves 28.6 dBm output power with 28.5% PAE is shown in Fig 7. Its die size including the drivers and PWPM generator is 1.3 x 1.6 mm$^2$. To the authors’ knowledge, this is the first switching PA in 65 nm CMOS, and it achieves the highest output power
in nanometer CMOS to date. It can be used to amplify signals with either non-CE with moderate (~6dB peak-minimum ratio) envelopes, or CE signals, without the use of a supply modulator.

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References:


Captions:
Fig. 1: Generalized PWPM PA.
Fig. 2: Schematic of the class-E PWPM PA.
Fig. 3: PA output power and PAE vs. input duty cycle (Freq = 2.2 GHz).
Fig. 4: Measured PA output power and PAE vs. frequency.
Fig. 5: Measured PA output with GMSK modulated input signal with symbol rate = 270 kHz. P_{out} = 27.5 dBm.
Fig. 6: Measured PA output with π/4-DQPSK modulated input signal with symbol rate = 192 kHz. P_{out}=26.7 dBm.
Fig. 7: Chip microphotograph in 65 nm CMOS.
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Fig. 7: Chip microphotograph in 65 nm CMOS.