A Class-G Supply Modulator and Class-E PA in 130 nm CMOS

Jeffrey S. Walling¹, Student Member, IEEE, Stewart S. Taylor², Fellow, IEEE and David J.
Allstot¹, Fellow, IEEE

¹Dept. of Electrical Engineering, Univ. of Washington, Seattle, WA 98195
²Intel Corp., Hillsboro, OR 97124

Abstract—A class-G supply modulator utilizes parallel low dropout regulators (LDOs) that are controlled by comparators and negative feedback. It optimizes the power consumption of a non-linear power amplifier (PA) operating with supply modulation, such that it draws current from one of multiple appropriately-sized supply voltages as determined by the input signal envelope. The class-G modulator is used in conjunction with a class-E PA operating in an envelope elimination and restoration (EER) mode to efficiently amplify signals with large peak-to-average ratios. The measured maximum output power and PAE are 29.3 dBm and 69%, respectively. The class-G technique is demonstrated for a 64 QAM, OFDM input signal (symbol rate = 4 μs) wherein the measured error vector magnitude (EVM) is 2.5% with an average efficiency of 22.6%.

Index Terms—Power Amplifier, Class-G, Class-E, Linearization, Supply Modulation, Envelope Elimination and Restoration, EER, Power Added Efficiency, Average Efficiency

Contact Information:
Jeffrey S. Walling
Dept. of Electrical Engineering, Univ. of Washington
Campus Box 352500, Seattle, WA 98195
Phone: 425-471-0081
Email: noyade@u.washington.edu

I. INTRODUCTION

Delivering near-watt output power in a fine-line CMOS power amplifier (PA) is difficult to achieve with high efficiency owing to scaling of the power supply voltage with minimum feature size. A typical PA must interface with either an antenna or filter with a characteristic impedance of 50 Ω, whereas it requires an optimum termination impedance of ~1-5 Ω for watt-level power output. In order to present the optimum termination to the PA, either a passive matching network is employed or a combining circuit is used to sum the outputs of several lower power PAs [1,2]. In the former, significant losses are incurred in the matching network due to the lossy on-chip passives such as spiral inductors and MIM capacitors. In the latter, the die area required for the combiner can be prohibitive, and can additionally incur significant loss owing to coupling to the lossy CMOS substrate.

A linear PA is designed to deliver significant output power to a load with high efficiency; however, it only achieves high efficiency when operating near its peak, or saturated output power level. This is troublesome because modern communications systems employ multicarrier modulation standards such as orthogonal frequency division multiplexing (OFDM), wherein the statistics of the envelope of the signal are such that the PA rarely operates near saturation [3]. Moreover, a PA for such a system must also behave linearly over a wide dynamic range, which typically requires that it operate in a backed-off state from its saturated output power level (e.g., $P_{out,max} = (P_{1\text{-}dB} - 3 \text{ dB})$).

A switching PA (e.g., class-E) achieves high efficiency because it exploits the switching characteristics of CMOS transistors in combination with a simple output network that comprises only a few passive elements. Unfortunately, it has a limited sensitivity to variations in input amplitude and often requires a means of linearization.
One design option that addresses these issues follows from the observation that a switching PAs has some sensitivity to the width of the pulse at its input. Hence, a system using pulse-width and pulse-position modulation may be used to linearize it, but the minimum pulse width that can be processed limits its dynamic range. One example of such a system fabricated in 65 nm CMOS processes pulse-widths as narrow as 40 ps, which enables processing of signals with peak-to-minimum ratios of 6-10 dB [4]; but, this dynamic range is smaller than required for systems employing OFDM, such as 802.11a and WiMax.

Another design option notes that the output power, $P_{out}$, of a class-E PA is given by:

$$P_{out} = 0.577 \frac{(V_{DD}-V_{sat})^2}{R_L}$$

(1)

where $V_{DD}$ is its supply voltage, $V_{sat}$ is the saturation voltage of the switch, and $R_L$ is the load resistance. From (1), it is clear that the class-E PA output power is proportional to the square of the supply voltage. A system that uses supply modulation such as envelope elimination and restoration (EER) linearizes the switching PA and offers a significantly larger dynamic range, but, the design of supply modulators with high efficiency then becomes a challenge. Many systems have been reported that use some variant of EER including some that directly modulate the power supply voltage [5,6,7,8,9], and others that effectively modify the resistance of the switching device [10,11].

In the former case, the supply modulator is designed using either a linear supply modulator [5,6,8], or a hybrid supply modulator that comprises linear supply and switching supply modulators [7]. In either scheme, the efficiency of the supply modulator is critical to the overall efficiency of the system. This paper introduces a CMOS class-G linear modulator, which operates with two different power supplies; hence, the PA operates from the smaller (larger) power supply voltage when the input signal amplitude is smaller (larger) than a predetermined
threshold. Consequently, the supply modulator is much more efficient as a result of dynamically changing the power supply voltage only when the signal properties demand.

This paper is organized as follows: efficiency enhancements associated with both single- and dual-supply modulators operated in an EER mode are described in Section II. In Section III, circuit design considerations for the class-G modulator along with the class-E PA are presented. Experimental results for a complete prototype class-G modulator and class-E PA designed in 130 nm CMOS are revealed in Section IV, and conclusions are given in Section V.

II. SUPPLY MODULATION

Envelope elimination and restoration was first proposed in 1952 (Fig. 1) as a way to linearize non-linear amplifiers [12]. In Kahn’s approach, an RF input signal is processed by two parallel paths. In one path, the envelope of the RF signal is “eliminated” using a limiting amplifier that removes any amplitude modulation. In the other path, it is detected, amplified, and applied to the PA as its power supply voltage. The beauty of Kahn’s method is that it allows the phase modulated signal to be amplified with high efficiency using a saturated PA such as class-D, class-E, or class-F. Whereas the original system was analog in nature, as shown, a modern implementation of the system can construct the envelope and phase signals using DSP techniques, which eliminates the envelope detector and limiting amplifier (Fig. 2).

A. Efficiency

Before considering the benefits of supply modulation, two definitions that are typically used in quantifying the efficiency of power amplifiers are reviewed; namely, drain efficiency and power added efficiency (PAE) [13]. Drain efficiency, $\eta$, is the ratio of the output power, $P_{out}$, to the DC power drawn from the supply, $P_{DC}$:
\[ \eta = \frac{P_{\text{out}}}{P_{\text{DC}}} \]  

(2)

This definition ignores power associated with driving the input of the PA; however, it is useful in determining the ideal efficiency of a system for comparison to others, and is used throughout the remainder of Section II.

For the final system design, a more accurate form of efficiency that takes into account power consumed by the driver, biasing, and overhead of the linearization scheme should be chosen. Overall PAE is chosen for this metric, and is used throughout Section IV:

\[ \text{PAE} = \frac{P_{\text{out}}}{P_{\text{DC}} + P_{\text{in}}} \]  

(3)

Finally, the previous efficiency definitions can be used to find the average efficiency, which is useful for measuring the efficiency when the RF signal has a time-varying input amplitude (e.g., amplitude modulation)[3]. It is defined as the ratio of the average output power, \( P_{\text{out,avg}} \), to the average input power, \( P_{\text{in,avg}} \):

\[ \eta_{\text{avg}} = \frac{P_{\text{out,avg}}}{P_{\text{in,avg}}} = \frac{\int_{V_{\text{min}}}^{V_{\text{max}}} P_{\text{out}} p(V) dV}{\int_{V_{\text{min}}}^{V_{\text{max}}} P_{\text{in}} p(V) dV} \]  

(4)

wherein \( P_{\text{in,avg}} \) includes all AC and DC input power to the PA. To determine the average efficiency of the PA according to (4), the probability density function (PDF) of the envelope of the amplitude modulation is used to weight the input and output powers; the PDF represents the relative time of the envelope amplitude at a given level. Note that \( p(V) \) represents the envelope PDF.

B. Class-G (Dual-supply) Modulator

A modern DSP-intensive EER PA topology with a single-supply modulator is shown in Fig. 2, wherein the digital baseband input signal is converted from Cartesian to polar form using a
CORDIC engine [14]. The resulting phase modulated signal is upconverted and applied to the input of the PA. After D/A conversion, the amplitude modulated envelope signal drives a linear supply modulator that comprises an operational amplifier in negative feedback with a supply control and two large PMOS pass transistors, $M_1$ and $M_2$, that modulate the voltage supplied to the PA. The op-amp with negative feedback forces $V_o = V_i$, thus presenting $V_i$ as the supply voltage to the PA. Finally, the amplified envelope and RF signals are restored at the output of the PA as shown.

The drain efficiency of a single-supply modulator degrades linearly with decreases in the output voltage. However, if the supply voltage is decreased along with the output voltage, the drain efficiency is increased [15]. The system shown in Fig. 2, first proposed by Raab [16], uses two supply modulators in parallel, controlled such that the first (second) modulator operates from $V_{DD}/x$ ($V_{DD}$) when the envelope input magnitude is less (greater) than $V_{DD}/x$, where $x$ is a voltage scaling factor $> 1$.

The efficiency of the dual-supply modulator is determined assuming the supply modulators and RF PA are ideal. The output power of the modulator is:

$$P_o = V_o I_o$$  \hspace{1cm} (5)  

$$I_o = \begin{cases} I_{o,1}, & 0 < V_o < \frac{V_{DD}}{x} \\ I_{o,2}, & \frac{V_{DD}}{x} < V_o < V_{DD} \end{cases}$$  \hspace{1cm} (6)  

and its DC input power depends upon the power supply voltage:

$$P_{DC} = \begin{cases} \frac{V_{DD}}{x} I_{o,1}, & 0 < V_o < \frac{V_{DD}}{x} \\ V_{DD} I_{o,2}, & \frac{V_{DD}}{x} < V_o < V_{DD} \end{cases}$$  \hspace{1cm} (7)  

Hence, the efficiency of the system is given by:
Like the single-supply modulator, the maximum value of $V_o$ is $V_{DD}$; hence, its peak efficiency is 100%. Moreover, the drain efficiency of the second supply modulator is also 100% with $V_o = V_{DD}/x$. The class-E PA has an efficiency of 100% for all input signals so the overall drain efficiency of an ideal dual-supply modulated class-E PA is defined by (8).

It is instructive to compare a single-supply modulated class-E PA to a linear class-AB PA operating near the class-B mode, which has an efficiency given by [13]:

$$\eta = \frac{\pi V_o^2}{4V_{DD}^2}$$

Again, the maximum value of $V_o$ is $V_{DD}$ so the peak drain efficiency is $\pi/4 \approx 78.5\%$; the efficiency rolls off as the square of the output voltage.

The drain efficiency vs. input envelope amplitude for both the ideal class-G dual-supply modulated class-E PA and the ideal class-AB PA are compared in Fig. 3. The characteristic shown ($x = 2$) is for a small supply voltage of exactly half the large supply voltage. In practice, $x$ is determined by the PDF of the envelope signal. The average efficiency for a 64 QAM OFDM signal is plotted versus $x$ in Fig. 4, and is shown to be optimal for $x = 2.5$. Note that the class-G dual-supply modulated class-E PA has higher drain efficiency for all envelope voltages. The envelope PDF for a 64 QAM OFDM modulated signal is also plotted. In contrast to a single-supply modulator, the dual-supply modulator is more efficient where the PDF shows the most likely envelope values. The average efficiency of the class-G dual-supply modulated class-E PA ($x = 2$) with this PDF is 52% compared to only 8% for the class-AB PA.

The concepts applied to the class-G modulator can, of course, be extended to more than two power supplies; there will be diminishing returns in practice, however, as the power
consumed by the added control circuitry and PA drivers becomes more significant for decreasing envelope voltages. The dual-supply class-G modulated class-E PA offers a ~6X improvement in average efficiency for such a Rayleigh envelope PDF with a large peak-to-average ratio, and, a significant improvement, in general, for almost all envelope distributions.

III. CIRCUIT DETAILS

A top-level schematic of the complete class-G dual-supply modulated class-E PA (Fig. 5) shows that a signal with complex modulation is first processed by a Cartesian-to-polar conversion block that produces an amplitude modulated signal, $A$, and a phase modulated signal, $\phi$. The phase modulated signal is applied directly to the PA driver, which consists of a buffer amplifier and a tapered inverter chain. The output signal of the PA driver is then input to a class-E PA that uses cascodes and on-chip passives to form the class-E wave shaping network. At the same time, the amplitude modulated envelope signal is input to the dual-supply modulator and its output provides the PA supply voltage. All circuits are designed in a 130 nm, RF CMOS process with 8 metal layers, including a thick top metal (4 μm) and MIM capacitors.

A. Class-E PA

1) Class-E Output Stage

The well known class-E topology (Fig. 6) [17] consists of a net positive shunt susceptance, $B_{opt}$, at the drain of a MOSFET switch connected to a series resonant circuit that has a slight excess reactance, $X_{opt}$, at the frequency of operation. The design equations for the class-E stage are [18]:

$$Z_{opt} = R_{opt} + jX_{opt}$$  \hspace{1cm} (10)

$$R_{opt} = 0.577 \left(\frac{V_{DD}+V_{Sat}}{P_{out}}\right)^2$$  \hspace{1cm} (11)
The matching network consisting of $L_m$ and $C_m$ (Fig. 6) is used to transform the external load impedance (usually 50 $\Omega$) to $Z_{opt}$. The drain capacitance, $C_D$, is typically formed by adding a capacitor in parallel with the parasitic capacitance at the drain of $M_1$. The equations above assume $L_d$ is an RF choke, which contributes no susceptance at the drain of $M_1$.

It has been shown that the use of a finite inductance for $L_d$ reduces the voltage swing at the drain to less than the traditional 3.6 times the supply voltage [19,20]. To design with a finite inductance, it is best to view the elements at the drain as forming a net susceptance, rather than as separate inductances and capacitances. A finite inductor (capacitor) contributes a negative (positive) susceptance; thus, the design equations become:

$$B_{opt} = \frac{0.1836}{\omega_0 R_{opt}}$$  \hspace{1cm} (14)

$$B_{opt} = B_{Cd} - B_{Ld}$$  \hspace{1cm} (15)

where $B_{opt}$ is the optimum susceptance, and $B_{Cd}$ and $B_{Ld}$ are the susceptances of $C_d$ and $L_d$, respectively. There is no closed form expression for the value of $L_d$; thus, to determine the design values, a circuit simulator is used to monitor the shapes of the waveforms, while sweeping $L_d$ and tuning $C_d$ simultaneously to maintain the same net susceptance.

It is noted that it is desirable to operate from as large a voltage as possible in order to achieve high efficiency because this allows for a smaller impedance transformation in the output matching network. There is, however, a practical limit to how large this voltage can be due to transistor reliability. By using an optimally sized drain inductance, $L_d$, it has been shown that the peak voltage stress applied to the transistor can be reduced to 2.5 times the supply voltage [19].
To allow for a larger supply voltage, the switching transistor can be cascoded with a higher breakdown thick gate oxide transistor, which is commonly provided for chip interfaces in modern technology. By using this cascode, the peak drain voltage can be divided between the switching device and the cascoded device. In this design, a thin-gate, minimum-length transistor (L = 130 nm) is cascoded with a thick-gate oxide transistor (L = 250 nm). This allows the PA to operate from a supply voltage of up to 3.3V, while guaranteeing that no node is driven above two times the nominal supply voltage for the process, which is common practice in CMOS PA design [21]. The complete PA including the buffers and driver chains is shown in Fig. 7. Note that though the matching network in Fig. 7 is not identical to that in Fig. 6, it remains functionally identical; e.g., the tapped capacitor matching network consisting of $C_1$, $C_3$ and $L_3$ ($C_2$, $C_4$ and $L_4$) is used to present $Z_{opt}$ to the drain of the power amplifier and $L_1$ ($L_2$) is used in combination with the parasitic capacitance at the drain of $S_{IN}$ ($S_{IP}$) to present $B_{opt}$.

2) Buffer and Driver

The PA input is driven by a buffer amplifier, followed by an inverter chain with a taper factor of 2. The buffer (Fig. 8) is a fully-differential amplifier consisting of an input differential pair and a mode-locked active load. Mode-locking ensures that the amplifier is able to operate with signals up to 4 GHz; careful sizing of M3X and M4X prevents oscillation. The amplifier uses a simple resistive input match to provide a 50 Ω interface, which allows the PA to be tested in stand-alone operation. The buffer is only necessary for a stand-alone device; it is not required in a fully-integrated transmitter, wherein the PA is on-chip with the DSP, baseband, and up-conversion circuits.

Following the buffer is a seven-stage inverter chain with a taper factor of 2. Each stage of the inverter is a custom layout, designed to ensure speed while operating with minimum power
consumption. Tuning inductors (Fig. 7: $L_{in,n}, L_{in,p}$) are used at the inputs of the class-E PA to resonate some of the input gate capacitances. This allows a smaller driver chain to be designed, and sacrifices a small amount of area for lower power consumption.

B. Class-G Supply Modulator

Conceptually, the class-G modulator consists of two parallel linear modulators that receive the envelope as an input signal, and draw current from either a low- or a high-voltage power supply. As shown in Fig. 9, the modulators comprise parallel low dropout regulators consisting of the operational amplifier and transistor pairs, $OA_1, M_1$ and $OA_2, M_2$ that are digitally controlled using comparators ($C_1$-$C_4$) and transmission gates ($S_1$-$S_4$). In typical operation, the comparators receive reference voltages, $V_{\text{ref,small}} > V_{\text{ref,big}}$. As the input voltage ($V_{in}$) is varied, the output current is initially sourced from transistor $M_1$, with the output voltage ($V_{out}$) fed back to the comparators. When $V_{out} > V_{\text{ref,big}}$, the pass transistor $M_2$ receives a signal, delayed by the pole associated with $R_2$ and its gate capacitance, which turns it on. As $V_{out}$ continues to increase until $V_{out} > V_{\text{ref,small}}$, $M_1$ receives a signal, delayed by the pole created by $R_1$ and the its gate capacitance, which turns it off.

The delays are necessary to ensure a transition period when current is always sourced to the load. Care must be taken that the load impedance is always significantly smaller than the impedance looking into either pass transistor so that crowbar current does not flow from $V_{\text{DD,big}}$ to $V_{\text{DD,small}}$. The values of the poles frequencies associated with $R_1$-$M_1$ and $R_2$-$M_2$ are found by experiment to be ~$1/2$ the maximum bandwidth of the input signal. In addition to the sizing of $R_1$-$M_1$ and $R_2$-$M_2$, the values of resistors $R_3$ and $R_4$ must be considered. They should be sized so that the highest swing at the input causes the output to approach saturation. In this system, a gain of ~3 was necessary, so $R_3 \approx 2R_4$. 
Timing and voltage levels of the critical signals at nodes $W$, $X$, $Y$ and $Z$, along with the current waveforms drawn from supplies $V_{DD}/x$ and $V_{DD}$, $i_s$ and $i_B$ (Fig. 9) are shown in Fig. 10. Note that a supply transition occurs around 1 μs, when the comparators $C_3$ and $C_4$ cause the voltage at $W$ to switch on $S_4$ and switch off $S_3$, thus allowing $OA_2$ to start to take control of the loop while transistor $M_2$ begins to conduct and $M_1$ is gradually turned off. At ~1.05 μs, the comparators $C_1$ and $C_2$ cause the voltage at $X$ to switch off $S_2$ and switch on $S_1$, causing all current to be sourced by transistor $M_2$. As the envelope voltage is reduced, first comparators $C_1$ and $C_2$ cause the voltage at $X$ to switch on $S_2$ and switch off $S_1$, and then $C_3$ and $C_4$ cause the voltage at $W$ to switch off $S_4$ and switch on $S_3$. This results in the current being sourced entirely through $M_1$ again.

The low dropout regulators each include an operational amplifier and a pass transistor (e.g., $OA_1$ and $M_1$). The op-amp is a folded-cascode stage with a Wilson current mirror active load. This design choice was made for two reasons: First, it was desirable to achieve all of the necessary gain in a single stage, and the Wilson mirror provides larger output impedance than a cascode mirror, for the same output swing. Second, the system requires a gain of only ~30 dB and a bandwidth greater than 30 MHz to meet performance specifications; using more stages to increase gain introduces stability concerns, reduces the bandwidth, and adversely impacts the efficiency due to the additional biasing. The closed-loop gain of the op-amp is shown in Fig. 11 exceeds the desired specifications over the range of input conditions.

The CMOS comparator used in the class-G circuit is a conventional configuration [22]. Hysteresis is used to limit switching due to noise when the input signal is near the threshold level. The comparators drive standard CMOS gates that select either $M_1$ or $M_2$, and thus determine which power supply sources current to the PA.
To demonstrate the functionality of the class-G modulator, a signal envelope derived from a 64 QAM OFDM modulated source is input to the modulator and the current drawn from each supply along with the output voltage is monitored (Fig. 12). To demonstrate the reduction in the glitch when a switching pole is added, the waveforms are plotted with and without the switching pole.

IV. EXPERIMENTAL RESULTS

Shown in Fig. 13 is a chip microphotograph of the prototype PA fabricated in a 130 nm RF CMOS process with 8 layers of metallization; including probe and bond pads, the complete class-G dual-supply modulated class-E PA of Fig. 5 uses a die area of 2 mm × 2 mm. Note that this is dominated by pad area, as the active circuitry only consumes an area of 1.6 mm × 1 mm; hence, substantial die area would be saved in a fully-integrated version. The class-G supply modulator that supplies power to the class-E PA operates from two different supply voltages, nominally 3.3V and 1.65V, whereas the PA driver operates from 1.5V. The PA delivers 29.3 dBm into 50 Ω, and achieves its maximum power added efficiency at 2 GHz.

The output power and PAE of the PA are plotted versus the square of the input voltage amplitude in Fig. 14. As expected, they increase with the square of the input envelope amplitude. The PAE characteristic is of particular interest, as it has a steeper slope and a secondary peak while operating from the small supply voltage (1.65V). The output characteristic has some nonlinearity with respect to the input envelope (AM-AM in Fig. 14 and AM-PM in Fig. 15), but this is correctible using pre-distortion techniques.

The quality factor of the output matching network is relatively low (~2-3); correspondingly, the frequency response of the PA allows for good output power and PAE over a wide range of frequencies as illustrated in Fig. 16. The -3 dB bandwidth of the PA is almost 2
GHz. The upper frequency limit is constrained by the speeds of the buffer amplifier and PA driver.

The class-G modulated class-E PA is designed to efficiently amplify signals with large peak-to-average ratios. To validate its performance, an OFDM signal with 64 subcarriers individually modulated with 64 QAM, with a symbol period of 4 μs, is applied to its input. The measured output constellation and normalized power spectral density (avg. power = 19.6 dBm, input frequency = 2 GHz) are shown in Figs. 17 and 18, respectively. The measured EVM is 2.5%. For comparison, the measured PSD is evaluated against the IEEE 802.11a spectral mask, and shown to exceed the specification for all frequencies.

The motivation for using a class-G EER transmitter is to increase the average efficiency. The PAE characteristic vs. input envelope is again plotted in Fig. 19. The average efficiency for a signal with the distribution shown is computed by weighting the PA output and input powers by the PDF and integrating over the input range. The calculated average efficiency is 24.5%. For comparison, the measured average efficiency for the same signal of 22.6% is superior to the ideal average efficiency of a linear PA. It should be noted that the efficiency does not include loss in generating the voltage supplies. However, modern switching supply regulators achieve efficiencies > 90% and in a typical situation these supply voltages are already available.

V. CONCLUSIONS

A class-G dual-supply modulated class-E PA that realizes efficient envelope restoration by operating from a large voltage supply only when the signal envelope requires is presented. Using the class-G modulated class-E PA enables efficient amplification of signals with moderate to large peak-to-average ratios (≈3-20 dB). The design methodology for a class-E PA with a class-G modulator is described and theoretical calculations for efficiency enhancement are presented.
A prototype circuit fabricated in 130 nm CMOS achieves a peak output power and PAE of 29.3 dBm and 69%, respectively. The design as validated by applying a 64 QAM OFDM-modulated signal to the amplifier (avg. power = 19.6 dBm), which achieves very good EVM (2.5%) and average efficiency performance (22.6%). A comparison to other supply modulated PAs is given in Table 1.

REFERENCES


Fig. 1. Kahn EER transmitter.

Fig. 2. Generic DSP-intensive EER transmitter topology with a dual-supply modulator.

Fig. 3. Drain and average efficiency comparisons for a dual-supply EER PA vs. a class-AB PA.
Fig. 4. Average efficiency vs. supply voltage scaling factor, $x$, calculated for a 64 QAM OFDM envelope PDF.

Fig. 5. Top-level topology of the class-G modulated class-E PA; note the input shows an analog representation of a digital input.

Fig. 6. Typical class-E PA.
Fig. 7. Class-E PA and driver.

Fig. 8. PA input buffer.
Fig. 9. Class-G supply modulator.
Fig. 10. Class-G modulator control waveforms.
Fig. 11. Simulated closed-loop gain of the dual-supply modulator.
Fig. 12. Simulated typical Class-G modulator from top: current waveforms with no switch pole, current waveforms with a switch pole, output voltage waveforms.
Fig. 13. Class-G dual-supply modulated class-E PA microphotograph in 130 nm CMOS.

Fig. 14. Measured class-G PA output power and PAE vs. input envelope.
Fig. 15. Measured AM-PM distortion.

Fig. 16. Measured class-G PA output power and PAE vs. frequency.
Fig. 17. Measured constellation for a 64 QAM OFDM-modulated input signal (avg. power = 19.6 dBm, frequency = 2 GHz).

Fig. 18. Measured PSD for a 64 QAM OFDM-modulated input signal (avg. power = 19.6 dBm, frequency = 2 GHz).
Fig. 19. Measured class-G average efficiency for 64 QAM OFDM-modulated signal (avg. power = 19.6 dBm, frequency = 2 GHz).

Table 1. Comparison to prior art

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*This design uses an off chip PA