Improving efficiency in CMOS Transmitters: Power Amplifier Trends and Challenges

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CMOS PA Trends: $P_{out}$

![Graph showing trends in output power (dBm) from 2000 to 2010. The graph includes data for Linear PA, Switching PA, and Power Combining.]
CMOS PA Trends: $P_{\text{out}}$

![Graph showing trends in power added efficiency over years for different types of power amplifiers: Switching PA, Linear PA, and Power Combining.](image-url)
Spectral vs. Energy Efficiency

Fundamental tradeoff: Spectral Efficiency vs. Energy Efficiency

1901 Marconi Transatlantic
1918 Armstrong Heterodyne
1933 Armstrong FM
1938 Chireix PA
1952 Kahn Transmitter
1978 FM Exceeds AM
1998 CMOS EER

0 0.2 0.4 0.6 0.8 1
Normalized Envelope (V)

0 10 20 30
Ocurrences (%)

1947 Point Contact Transistor (Shockley)
1960 MOS Transistor

1998 CMOS Class-G EER
2005 CMOS Hybrid EER
2008 CMOS EER

1/1/1979 Commercial Cellular (Japan)

0 0.2 0.4 0.6 0.8 1
Normalized Envelope (V)

0 5 10 15 20 25
Ocurrences (%)

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Variable vs Constant Envelope Modulation - I

I(t) and Q(t) enter the I-Q Modulator. The outputs of the modulator are $\sin(\omega_{LO}(t))$ and $\cos(\omega_{LO}(t))$. These signals are then amplified by a Power Amplifier. The output signal is a combination of constant envelope modulation and variable envelope modulation. Constant envelope modulation results in signals like MSK and GMSK, while variable envelope modulation results in signals like BPSK, QPSK, and QAM.

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Variable vs. Constant Envelope Modulation - II

Variable Envelope Modulation

- BPSK, QPSK, QAM

- Fluctuations in signal amplitude
  ⇒ Possible IM products

- Linear PA required
  ⇒ Poor power efficiency

Constant Envelope Modulation

- MSK, GMSK

- Needs larger BW
  ⇒ Poor spectral efficiency

- Efficient non-linear PA possible (Class C, D, E, F)
Energy Efficiency Issues

Linear PA

Envelope Following PA
Outline

- Transmitter (Tx) Architectures
- CMOS Power Amplifier Considerations
- Class-G Transmitter
  - System Limitations
  - 130nm Implementation
Transmitter Architectures

- **Mixer-based**
  - Direct-Conversion
  - Two-step
  - Harmonic rejection

- **PLL-based**
  - Offset PLL
  - Open loop modulation
  - Two-point modulation
  - Closed loop modulation
TX Evolution: Mixer Based

**Constant Envelope Modulation**

- MSK, GMSK

**Variable Envelope Modulation**

- BPSK, QPSK, QAM

**IQ Modulator**

- \( I(t) \)
- \( Q(t) \)
- \( \sin \omega_{LO}(t) \)
- \( \cos \omega_{LO}(t) \)

**Linear PA**

**Band Select Filter**

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Mixer-based Transmitters

• Most common
  - Simple to implement
  - Supports Constant/Variable envelope modulation

• Mostly analog
  - Low spurious noise
  - Off-chip high-Q, low-distortion, low-noise Band Select Filter
  - High cost of implementation ($1-2 Front End Module)
  - Need Linear (often off-chip) PA
TX Evolution: PLL Based

PLL Modulator

- Phase Freq Detector
- Charge Pump / Loop Filter
- ΔΣ Frac-N
- VCO
- Switch PA
- φ(t)

Constant Envelope Modulation → MSK, GMSK

Variable Envelope Modulation → BPSK, QPSK, QAM
PLL-based Transmitters

- More Digital
- Easy (relatively) integration
- Reduced or Removed Post-PA Filtering $\Rightarrow$ save power (loss)
- Inherent filtering action of PLL
- Supports only Constant Envelope Modulation
TX Evolution: Polar (PLL Based)

Variable Envelope Modulation
→ BPSK, QPSK, QAM

Constant Envelope Modulation
→ MSK, GMSK

PLL Modulator

Supply Modulator

Switch PA

ΔΣ Frac-N

Charge Pump / Loop Filter

Phase Freq Detector

A(t) → BPSK, QPSK, QAM

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Polar Transmitter - Advantages

- PA saturated $\Rightarrow$ Higher efficiency $\Rightarrow$ Low Heat Dissipated
- Saturated PA $\Rightarrow$ stable with varying load
- CMOS $\Rightarrow$ Can Use Switching PAs
- Much circuitry realizable using digital gates
- Adaptable to multi-mode, multi-band transmitters
- Bandwidth expansion of Amplitude/Phase components
- AM/AM and AM/PM Distortion
- Time alignment of the AM and the PM signal paths needed

Outline

• Transmitter (Tx) Architectures
• CMOS Power Amplifier Considerations
• Class-G Transmitter
  ➢ System Limitations
  ➢ 130nm Implementation
CMOS PA Considerations

- Output Power ($P_{out}$)
  \[ P_{out} = \frac{(V_{DD} - V_{sat})^2}{2R_{opt}} \]
- 65nm: 1W, $V_{DD}$=1.2, $V_{sat}$=0.2 $\rightarrow$ $R_{opt}$=0.5Ω
- Power Added Efficiency (PAE)
  
  Class A: 
  \[ \eta = \frac{V_{out}}{2V_{DD}} \rightarrow 0.5 \]
  Switching: $\eta \rightarrow 1$
  
  Class AB: 
  \[ \eta = \frac{\pi}{4} \left(\frac{V_{out}}{V_{DD}}\right)^2 \rightarrow 0.785 \]
Linear vs. Switching PA

- Linear PA
  - MOS as amplifier
  - Varying envelope
  - Poor Efficiency
  - Thermal stress
- Switching PA
  - MOS as switch
  - Constant envelope
  - Good Efficiency
  - Voltage stress
Linear PA (Class-B)

- Bias for half-cycle conduction
- Peak $\eta = 78.5\%$
- Need high-Q filter
- Thermal stress

$$R_{opt} = \frac{V_{DD}^2}{2P_{out}}$$
Switching PA (Class-E)

- Zero Voltage Switching
  - Rise in $v_D$ delayed until switch off
  - $v_D = 0$ @ switch on
  - $dv_D/dt = 0$ @ switch on

- Ideal $\eta = 100\%$

- Voltage Stress
Voltage Stress (Class-E PA)

- Stress – $v_D \sim 3.6V_{DD}$
  - M1 off $\rightarrow$ No "hot carrier" effect
  - Oxide Breakdown $\rightarrow V_{DG}$ large
- $V_{stress} < 2V_{DD,nom}$

<table>
<thead>
<tr>
<th>Maximum Voltage Stress</th>
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</thead>
<tbody>
<tr>
<td><strong>Switch “On”</strong></td>
</tr>
<tr>
<td>$V_{DD,DR}$</td>
</tr>
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</table>

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Voltage Stress Mitigation

- Distribute voltage to reduce stress
- Thick-gate device > Stress tolerance
- Finite supply inductance → reduced peak $v_D (\sim 2.5V_{DD})$

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Outline

• Transmitter (Tx) Architectures
• CMOS Power Amplifier Considerations
• Class-G Transmitter
  ➢ 130nm Implementation
  ➢ System Limitations
• EER = Envelope Elimination and Restoration
  ➢ For saturated amplifier, $P_{out} \propto$ PA Supply Voltage
  ➢ Can be mostly digital
LDO Supply Modulator

- $V_{out} \approx ENV_{in}$

- $P_{OUT} = i_{OUT} v_{OUT}$

- $P_{DC} = i_{OUT} V_{DD}$

- $\eta$ is proportional to $v_{out}$

- $\eta = \frac{P_{OUT}}{P_{DC}} = \frac{v_{OUT}}{V_{DD}}$

- Peak $\eta = 100\%$

LDO = Low Dropout Regulator
LDO Supply Modulator Efficiency

- Overall Efficiency is product of supply modulator and PA
- Single supply \( \rightarrow \) improvement over Linear PA
Dual Supply Modulator (Class-G)

• Small envelope use Vdd/x (peak $\eta = 100\%$ @ $Env_{in} = Vdd/x$)
• Large envelope use Vdd (peak $\eta = 100\%$ @ $Env_{in} = Vdd$)
• Extend to more than two supplies?
Modulator Efficiency (Class-G)

- Overall Efficiency is product of supply modulator and PA
- Ideally 5X higher average $\eta$ than linear PA for this PDF
Class G: Avg. $\eta$ vs. Threshold ($x$)

![Graph showing the normalized threshold vs. average efficiency for different technologies.]

- 64 QAM, OFDM
- Bluetooth EDR
- WCDMA
- 802.11a

Normalized Threshold (V)

Avg. Efficiency (%)
Class-G Implementation

- Supply Modulator and PA → in CMOS
- Envelope and Phase Modulation → off chip
Class-G Modulator

- Dual-loop LDOs
- \( V_{in} < V_{\text{thresh}} \rightarrow \text{output from } V_{DD/x} \)
- \( V_{in} > V_{\text{thresh}} \rightarrow \text{output from } V_{DD} \)
Bandwidth Limitation

- Margin-to-Mask (dB)
- EVM-rms (%)
- Frequency Offset (MHz)
- Norm. Output Power (dB)

- FCC
- Mask
- Signal

- Bandwidth Limitation

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Typical Glitch (Class-G)

Output Envelope

- Y-axis: Output Voltage (V)
- X-axis: Time (µs)

Output Current

- Y-axis: Output Current (A)
- X-axis: Time (µs)

- Graphs show comparison between small and big currents with and without switch pole.
Glitch Limitation

EVM-rms (%)  Margin-to-Mask (dB)

Normalized Glitch Amplitude ($V_{\text{thresh}}$)

Normalized Glitch Duration ($T_{\text{sym}}$)

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Class-E PA and Driver

- Interstage tuning inductors reduce driver power
- Driver taper of 2 – custom stages
130nm Class-G PA

- 3.3 V Supply Modulator
- PA Output Stage
- PA Driver Stage
- Interstage Tuning Inductor
- 1.65 V Supply Modulator
Class-G Static Measurements

Freq = 2 GHz

64 QAM, OFDM, Symbol Period = 4µs
- = theory avg. PAE (24%)
= measured avg. PAE (22%)
Class-G Dynamic Measurement

rms EVM = 2.5%

Freq = 2 GHz

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• 4X increase in avg. PAE=22.6% (linear PA, 64 QAM, OFDM avg. PAE~5%)
• Measured EVM (64 QAM, OFDM)=2.5%
# Class-G Comparison to Prior Art

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Peak Pout (dBm)</th>
<th>Peak PAE (%)</th>
<th>Avg. PAE (%)</th>
<th>EVM-rms (%)</th>
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<td>30</td>
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<td>7</td>
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Walling, et. al., RFIC 2009
Walling, et. al., JSSC, September 2009
Outline

• Transmitter (Tx) Architectures

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• Class-G Transmitter
  ➢ 130nm Implementation
  ➢ System Limitations
Polar/EER Limitations

- Bandwidth Expansion
- Time Alignment
- Supply Glitch

\[ A(t) = \sqrt{I^2(t) + Q^2(t)} \]

\[ \phi(t) = \tan^{-1}\left(\frac{Q(t)}{I(t)}\right) \]
Delay Mismatch Effects

- All delays are normalized to the signals symbol period
  - Bluetooth EDR $T_{sym} = 1 \mu s$
  - WCDMA $T_{sym} = 260$ns
  - IEEE 802.11a $T_{sym} = 50$ns
- Specifications are met for delay mismatches < 0.065$T_{sym}$, 0.06$T_{sym}$ and 0.04$T_{sym}$
Finite Bandwidth Effects: 802.11a

- All bandwidths are normalized to one RF Bandwidth ($BW_{RF}$)
  - IEEE 802.11a $BW_{RF}=20$MHz
- Specifications are met for delay mismatches $A, \phi$ BW $> 2.5BW_{RF}$
Finite Bandwidth Effects: WCDMA

- All bandwidths are normalized to one RF Bandwidth ($BW_{RF}$)
  - WCDMA $BW_{RF}=3.84$MHz
- Specifications are met for delay mismatches $A BW > 2.5BW_{RF}$, $\phi BW > 1.75BW_{RF}$
Finite Bandwidth Effects: Bluetooth EDR

- All bandwidths are normalized to one RF Bandwidth ($BW_{RF}$).
- Bluetooth EDR $BW_{RF}=1$MHz.
- Specifications are met for delay mismatches $A BW > 1.75BW_{RF}$, $\phi BW > 1.5BW_{RF}$.
Glitch Effects: 802.11a

- All bandwidths are normalized to one RF Bandwidth (BW\text{RF})
  - IEEE 802.11a \( T_{\text{sym}} = 50\text{ns} \)
  - Specifications are met for glitches < 0.05\( T_{\text{sym}} \) and 0.5\( V_{\text{thresh}} \)
Glitch Effects: WCDMA

- All bandwidths are normalized to one RF Bandwidth ($BW_{RF}$)
  - WCDMA $T_{sym} = 260$ns
- Specifications are met for glitches $< 0.025T_{sym}$ and $0.5V_{thresh}$
Glitch Effects: Bluetooth EDR

- All bandwidths are normalized to one RF Bandwidth \( (BW_{RF})_{sym} \)
- Bluetooth EDR \( T_{sym} = 1 \mu s \)
- Specifications are met for glitches < 0.05\( T_{sym} \) and 0.6\( V_{thresh} \)
Conclusions

• Polar Loop and EER Transmitters offer great potential to enhance TX and PA overall efficiency
• Important for ever increasing demand for mobile data rate and desire to be untethered
• Class-G extends the benefits of EER, at almost no cost→most platforms already include multiple supply voltages
• Limitations are difficult to meet, but quantifiable→scaled CMOS will ultimately help to meet difficult bandwidth and timing issues