Low Phase Noise CMOS Voltage-controlled Oscillators

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Abstract—Design considerations and performance comparisons for several low phase noise CMOS voltage-controlled oscillator (VCO) topologies are presented including the Hartley, quadrature Colpitts, Clapp, and tuned-input tuned-output configurations. An indirect approach for high-frequency signal generation using a VCO coupled with a 2X passive frequency multiplier is also described. Several of the structures are attractive alternatives to the conventional LC tank VCO.

Index Terms—Voltage-controlled oscillator, Hartley oscillator; Colpitts oscillator; Clapp oscillator; dual-tank oscillator, tuned-input tuned-output oscillator; phase noise transformer.

I. INTRODUCTION

Achieving excellent noise performance is one of the foremost requirements for a CMOS receiver front end. In such a system, a voltage-controlled oscillator (VCO) is employed in a frequency synthesizer to generate the local oscillator (LO) signal that drives the receive mixer. The phase noise of the VCO directly affects the spectral purity of the received signal in many ways, especially when used in a low loop-bandwidth synthesizer. The cross-coupled LC oscillator is one of the most widely used circuit configurations in modern CMOS implementations. However, the need to continuously reduce the phase noise of CMOS VCOs has led to active research of several other basic oscillator topologies.

A Hartley voltage-controlled oscillator that uses T-coil coupling is proposed in Section II. Section III reviews a quadrature Colpitts configuration, and Section IV describes a Clapp VCO. A fully-integrated CMOS implementation of a tuned-input tuned-output (TITO) VCO in a 0.18µm process is presented in Section V. Its theory of operation is presented including the frequency of oscillation as well as start-up and phase noise characteristics. Section VI describes the design and implementation of an indirect signal generation approach wherein a VCO frequency is multiplied by 2X using a passive mixer. All of the oscillator techniques presented compare favorably to the conventional LC VCO in terms of a standard figure-of-merit.

II. CMOS HARTLEY OSCILLATORS

Among alternative VCO topologies, the Hartley Oscillator (Fig. 1) has received relatively little attention. This is probably because its implementation requires either a tapped inductor, which is difficult to model and design, or two separate inductors, which require a relatively large chip area. Fully-differential designs are often even more difficult to design, as they typically use transformers, or even more inductors. On one hand, the conditions for oscillation contribute to a less reliable start-up characteristic than for the conventional cross-coupled configuration. On the other hand, the Hartley VCO, as with other LC tank-based oscillators, exhibits better cyclostationary noise properties [1].

Fig. 1. Hartley oscillator topology.

To determine the oscillation frequency and start-up conditions for a common-gate Hartley oscillator (Fig. 1), nodal equations at the source and drain are solved:

\[(V_s - V_d) Y_2 + V_s (g_m + Y_l) = 0\]  
\[(V_d - V_s) Y_2 + V_d Y_3 - V_s g_m = 0\]

If the inductors are assumed to be lossy wherein \(G_1\) and \(G_2\) represent their shunt conductances, then:

\[Y_l = G_1 + jB_1 = G_1 - j(1/\omega L_1)\]
\[ Y_2 = G_2 + jB_2 = G_2 - j(1/\omega L_2) \]  
(4)

\[ Y_3 = jB_3 = j\omega C_3 \]  
(5)

One solution for (1) and (2) is to set the drain and source voltages to zero; however, that solution is not acceptable in an oscillator where the determinant of the admittance matrix must be zero:

\[ g_m Y_3 + Y_1 Y_2 + Y_1 Y_3 + Y_2 Y_3 = 0 \]  
(6)

Solving for the real and imaginary parts of (6) yields the oscillation frequency and bounded start-up condition:

\[ \omega_0 = \sqrt{1/C_3(L_1 + L_2)} \]  
(7)

\[ g_m \geq \frac{X_1^2(R_1 + R_2) + R_1 R_2^2 + R_1^2 R_2}{R_1 R_2 (R_1 R_2 - X_1^2)} \]  
(8)

A differential topology (Fig. 2) is designed using T-coils rather than individual inductors in order to reduce the overall die area consumed by the spirals. \( M_1 \) and \( M_2 \) are the primary active elements whereas \( M_3 \) and \( M_4 \) are self-biased current sources [2].

\[ \text{Fig. 2. Hartley oscillator using T-coils.} \]

\[ \text{Fig. 3. Simulated phase noise of the Hartley oscillator.} \]

The Hartley oscillator of Fig. 2 is simulated using T-coil models obtained with \textit{ADS MOMENTUM}. It operates from 5.3-5.8GHz—a tuning range of 8.9%. The simulated phase noise is -129dBc/Hz @ 1MHz offset. It consumes 20mW and exhibits an \textit{FOM} of -191dBc/Hz, which is defined as:

\[ FOM = 10 \cdot \log_{10} \left( \frac{\omega_0}{\Delta \omega} \right)^2 \cdot \frac{1}{L(\Delta \omega) \cdot P_{\text{dc}} [\text{mW}]} \]  
(9)

where \( \omega_0 \) is the center frequency, \( P_{\text{dc}} \) is the DC power dissipation in mW, \( \Delta \omega \) is the offset frequency with respect to the carrier frequency, and \( L(\Delta \omega) \) the phase noise power spectral density.

\[ \text{III. QUADRATURE COLPITTS VCO} \]

Most monolithic RF voltage-controlled oscillators use LC resonators to achieve high spectral purity and cross-coupled MOSFET pairs for ease of design and reliable start-up. A drawback of the conventional topology is that thermal and flicker that are injected into the oscillator outputs at their zero crossings degrade phase noise performance. Because such switching does not occur at zero crossings in the Colpitts configuration, it is less susceptible to noise current injections and exhibits fundamentally superior noise performance [1][3][4].

One approach for quadrature signal generation uses a single VCO output and a passive RC-CR poly-phase filter. It requires large die area and is sensitive to quadrature phase mismatches that are strongly dependent on device matching and operating frequency. A second alternative combines a single VCO running at twice the frequency of interest with two divide-by-two flip-flops. This technique suffers from increased power consumption and sensitivity to the duty cycle of the VCO waveform [5]. An indirect synthesis approach is described later in this paper. Another option, anti-phase injection, achieves low phase noise and high quadrature phase accuracy [5]-[6]. Its primary drawback is doubled die area and power consumption.

\[ \text{Fig. 4. Quadrature Colpitts CMOS VCO.} \]
A QVCO capable of good noise performance and small quadrature phase mismatch is shown in Fig. 4. Each VCO is implemented as a differential Colpitts oscillator. The outputs of the QVCO are forced to oscillate 90° out of phase with the first VCO in-phase coupled to the second and the second anti-phase connected to the first. The coupling transistors \((M_3)\) are connected in series with the active \((-G_{m})\) devices \((M_2)\), but below them rather than as cascodes [6]. This eliminates large cascode transistors, and provides a wide tuning range and reliable start-up [7]. To minimize phase mismatches between the in-phase and quadrature outputs, the common-source nodes are connected. \(R_{bias}\) is used for biasing to reduce flicker noise up conversion, and \(L_2\) in series with \(R_{bias}\) provides high impedance at the second harmonic frequency.

Design of the QVCO begins with start-up—small-signal analysis shows that the minimum \(g_{mc}\) of \(M_1\) in Fig. 4 is:

\[
g_{mb} > g_{me} = 2\omega_0^2 C_1 C_2 R_s\tag{10}
\]

where \(\omega_0\) is the oscillation frequency and \(R_s\) is the loss resistance of the inductor [8]. A design margin of three is used to guarantee start-up. \(C_1\) and \(C_2\) are high-Q MIM capacitors, and the \(C_1/C_2\) ratio is 10 to reduce tank loading and increase tank voltage, thus reducing phase noise.

The impulse sensitivity function \((ISF)\) is a periodic function that defines sensitivity to an impulsive input; it is related to phase noise via:

\[
L(\Delta f) = 10 \log_{10} \left( \frac{i_n^2}{2 \cdot \Delta \omega^2} \cdot \frac{\Gamma_{\text{rms}}^2}{Q_{\text{max}}^2} \right) \tag{11}
\]

where \(\Delta \omega\) is the offset frequency from the carrier, \(i_n^2/\Delta f\) is the power spectral density of the current noise source, \(Q_{\text{max}}\) is the maximum charge swing, and \(\Gamma_{\text{rms}}\) is the rms value of the effective \(ISF\) [4]. Clearly, phase noise optimization requires \(ISF\) minimization. \(ISF\) for a Colpitts QVCO and a conventional QVCO are plotted in Fig. 5. Clearly, the \(ISF\) amplitude of the Colpitts oscillator is smaller than that of its negative resistance counterpart.

### IV. CLAPP VCO

Phase noise in an oscillator is improved by increasing the signal power relative to the noise power. In the Colpitts VCO, however, breakdown voltages of the active devices limit the swing at the oscillation node. Further improvement in phase noise by increasing signal swing dictates the use of an extra capacitor tap leading to the Clapp configuration. As illustrated in Fig. 7, the extra tap allows very large voltage swings across the inductor and the tapped divider. The swing across the transistor remains within the breakdown voltage limits [9].

The tank inductor in the Clapp oscillator can be connected to one of the three nodes of a transistor, leading to three different configurations. When connected to the drain or source, dc biasing problems are encountered. However, the source-follower Clapp is well-suited for a
CMOS implementation as in the fully-differential version of in Fig. 8. A center-tapped symmetrical inductor saves area and increases $Q$. The input impedance looking into the gate node from the $L$-$C_3$ branch is

$$Z_{in} = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} - \frac{g_m}{\omega^2 C_1 C_2}$$  \hspace{1cm} (12)

The negative term in (12) provides the negative resistance needed to compensate for the finite $Q$ of the inductor. The resonant frequency is:

$$f_{osc} = \frac{1}{2\pi \sqrt{L \cdot (C_{var} + C_{series})}}$$  \hspace{1cm} (13)

where $C_{series}$ is the series equivalent of $C_1$, $C_2$, and $C_3$, and $C_{var}$ represents the varactor. To enhance tuning range, $C_2$ can be replaced by a varactor; however, the improvement is limited because the effective series capacitance is dominated by $C_1$. Note that the diffusion terminal of a MOS varactor has a significantly lower $Q$ than its gate terminal. Since neither end of $C_3$ is connected to a common-mode point, implementing it with a varactor adversely affects start-up and phase noise characteristics.

Fig. 8 shows the fully-differential CMOS Clapp VCO. High-\(Q\) MIM capacitors are used to implement the tap capacitors, with an optimum ratio of 1:1.5:5 ($C_1$:$C_2$:$C_3$) for best phase noise performance. To obtain a large tuning range, $C_1$ (which dominates $C_{series}$) is kept small in comparison to the varactors.

A simulated phase noise plot at 6GHz is shown in Fig. 9. It shows phase noise spectral densities of $-98$dBc/Hz and $-123$dBc/Hz at offset frequencies of 100 kHz and 1 MHz, respectively. The current consumption is 5mA from 1.8V, and the tuning range is 18% (4.95-5.97GHz). It achieves an FOM of 189dBc/Hz @ 1MHz offset.

**V. TITO OSCILLATOR THEORY**

An implementation of a tuned-input tuned-output (TITO) CMOS VCO is shown in Fig. 10. A common-source amplifier with positive feedback action through the gate-drain capacitor, $C_f$, forms the basic TITO core. $L_g$ and $C_g$ constitute the main tank at the gate ($g$), and $L_d$ and $C_d$ form the auxiliary tank at the drain ($d$). Here, $C_g$ includes $C_{gs}$ of $M_I$ and other parasitic capacitances at the gate; the tuning capacitance of the auxiliary tank, $C_d$, includes $C_{ds}$ of $M_I$ and parasitics at the drain, and feedback capacitance, $C_f$, includes $C_{gd}$ of $M_I$. This CMOS implementation is derived from the classical tuned-grid tuned-plate oscillator [10].

Fig. 9. Simulated phase noise of the CMOS Clapp VCO.

**Frequency Offset (Hz)**

Fig. 10. A basic CMOS TITO oscillator.

Assuming $L_d = L_g = L$, and $C_d = C_g = C_v$, the frequency of oscillation is:

$$\omega_0 = \frac{1}{\sqrt{L \left( C_v + 2C_f \right)}}$$  \hspace{1cm} (14)

If the two resonant tanks have equal quality factors, the minimum transconductance required for start-up is:

$$g_{m,min} = G_d + G_g = 2G$$  \hspace{1cm} (15)

As the individual natural frequencies of the tanks, given by $\omega_k = \omega_d = 1/\sqrt{LC_v}$, are less than the frequency of oscillation (14), they act inductively at this frequency with their inductances enhanced due to tuning. In one sense, the superior performance of the TITO oscillator is attributable to this attribute. Representing the drain tank as $L_{d,eq}$ in series with tank resistance, $r_d$, at the oscillation frequency, the input admittance looking into the gate of the common-source transistor is:

$$\text{Re}\{Y_{in}\} \approx -g_m \omega_0^2 C_f \frac{L_{d,eq} - r_d C_f}{1 - \omega_0^2 L_{d,eq} C_f}$$  \hspace{1cm} (16)
This negative admittance compensates the loss in the gate tank and sustains oscillations in the core VCO circuit [11]. Not only the positive admittance (from $L_g$), but also the negative admittance (from $L_d$) depends on the $Q$ values of the inductors, unlike in other VCOs. A higher $Q$ enhances the negative input admittance, and thereby reduces power consumption and phase noise.

A TITO VCO resembles a Hartley or Colpitts oscillator with regards to its impulse sensitivity function [11] because most of the drain current flows only near the minimum of the tank voltage. Consequently, most of the drain noise is injected when the tank is insensitive to noise perturbations. Further improvement in the phase noise when compared to a Colpitts or Hartley VCO is attributed to the additional filtering action from the drain resonant tank. Compared to a standard cross-coupled VCO, a TITO VCO has superior phase noise performance at the expense of silicon area to accommodate a second inductor.

Fig. 11 shows the topology of a fully-differential CMOS TITO VCO [12]. $L_g$ and $L_d$ are realized as symmetric inductors to save area and increase their $Q$ factors. Identical varactors are connected across the auxiliary (drain) and main (gate) tanks to ensure that they tune together over the span of oscillation frequencies; the tank inductors are also kept similar in terms of layout details to maximize matching. $C_g$ and $C_d$ are implemented using MOS varactors to achieve frequency tuning. Based on (14) and (16), $C_f$ has an optimum value based on design tradeoffs between start-up reliability and tuning range. On one hand, a large value of $C_f$ ensures a large negative admittance and eases start-up. On the other hand, a large $C_f$ adversely affects the tuning range. In the final implementation, an explicit MIM capacitance of 1pF is added to account for the above tradeoff. Care is taken not to have an excessively high signal swing, as it leads to a distorted sinusoidal output voltage.

Fig. 7 shows a measured phase noise plot of the TITO VCO operating at 2.5GHz. At a 100kHz offset frequency, the phase noise is $-110$dBc/Hz, and at a large offset of 1MHz, it is $-130.5$dBc/Hz. The tuning range varies from 2.34GHz to 2.72GHz, giving a tuning range of 15.3%. The CMOS TITO VCO attains an FOM of 187.2dBc/Hz.

![Fig. 11. A fully-differential TITO VCO in CMOS.](image)

VI. INDIRECT FREQUENCY GENERATION

An indirect carrier generation method wherein a VCO core, operating at a relatively small fraction of $f_c$ where device gain is higher for a given power consumption, is followed by a passive mixer acting as a frequency multiplier to generate a high frequency LO without increased DC power dissipation has been developed [13].

To motivate the indirect method, consider a simplified equation for phase-noise [14]:

$$L(\Delta f) = \frac{1}{8Q^2} \frac{F}{P_{\text{sig}}} \left( \frac{f_0}{\Delta f} \right)^2$$  \hspace{1cm} (17)

where $L(\Delta f)$ is the single-sideband phase noise in dBc/Hz as a function of offset frequency from the carrier, $Q$ is the loaded resonator quality factor, $P_{\text{sig}}$ is the signal power in Watts, and $F$ is the oscillator noise factor.

Equation (17) shows that options to reduce phase noise at high frequencies include increasing $Q$ and/or DC power consumption. Tank quality factor, $Q_{\text{tank}}=\left(1/Q_L + 1/Q_C\right)^{-1}$, depends on both inductor $Q_L$ and varactor $Q_C$. $Q_C=\omega C/R_S$ increases with frequency, whereas $Q_L=R_p/\omega C$ decreases. $Q_{\text{tank}}$ is degraded by reduced $Q_C$ (due to non-quasistatic effects) and $Q_L$ (due to enhanced skin and proximity effects), especially at frequencies $>20$GHz.

Equation (17) also shows that a 2X multiplication of the fundamental frequency, with everything else staying the same, results in a 4X degradation of phase noise. Hence, indirect LO generation increases the phase-noise of the core fractional VCO by 6dBc/Hz, and the frequency multiplier also increases the phase-noise.

The primary advantage of the passive mixer over its active counterpart is that a passive mixer requires zero DC bias current which provides significant power savings. Furthermore, passive mixers have superior linearity.
compared to active mixers, which allows for higher output power levels from the core VCO.

Fig. 13: Measured phase noise plots for (a) combined VCO/mixer and (b) standalone 24GHz VCO.

Whereas active mixers contribute additive thermal and 1/f noise above that associated with the simple frequency multiplication, passive mixers suffer from conversion loss. The theoretical conversion loss of a passive mixer is 

$$20\log\left(\frac{2}{\pi}\right) = -3.9\text{dB}.$$ 

However, the excess phase noise of a mixer is low compared to an on-chip direct LO, so passive and active mixers are comparable in this respect [15].

To quantify the advantages of the indirect approach, a standalone 24GHz VCO is compared to a 12GHz VCO cascaded with a 2X passive mixer. Both VCOs use the complementary cross-coupled topology. A differential tuning scheme minimizes AM-to-PM conversion owing to common-mode noise on the control line.

All circuits are fabricated in a 6-metal 0.18μm CMOS process having an $f_{\text{max}}$ of 45GHz. The VCOx2 consumes 5mA from a 2.2V supply while the standalone 24GHz VCO consumes 15mA from a 3.0V supply. Both circuits are wafer probed with the outputs taken single ended which results in a 3dB loss of output power. A total power loss of 8dBm is measured in the test setup at 24GHz. Where appropriate, these losses are accounted for in subsequent results.

The measured tuning range for VCOx2 and the standalone 24GHz VCO is 3GHz and 1.5GHz, respectively. The measured gain of VCOx2 and the standalone 24GHz VCO is 1.24GHz/V and 424GHz/V, respectively. The wider tuning range of the VCOx2 owes to the smaller contribution of parasitic capacitances to the total tank capacitance. The measured phase noise values of the VCOx2 (Fig. 13(a)) at offsets of 100kHz, 1MHz, and 3MHz are -75.5, -99.1, and -105.1dBc/Hz, respectively. For identical offsets, the standalone 24GHz VCO (Fig. 13(b)) has measured phase noise values of -85.2, -98.9, and -105.3dBc/Hz, respectively.

It is seen that the indirect method gives a 6dB improvement in FOM over the direct method for equal phase noise. Comparison with other oscillators using the figures-of-merit also validates this design methodology.

**REFERENCES**


