A 28.6dBm, 65nm Class-E PA with Envelope Restoration by Pulse-Width and Pulse-Position Modulation

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Outline

• Motivation
• Bandpass Pulse Modulation
• PWM Combiner/Driver Design
• Class E PA Design
• Measurement Results
• Conclusions
Motivation - I

- Many envelope PDFs are Rayleigh
Motivation - I

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- Desire a PA with high efficiency at backoff
Motivation - I

- Many envelope PDFs are Rayleigh
- Desire a PA with high efficiency at backoff
- Switching PAs
  - Good efficiency
  - Need envelope restoration
Motivation - II

- **EER**
  - Time align difficult
  - Need DAC and supply modulator
  - Good dynamic range

- **Outphasing**
  - Need 2 PAs
  - Combiner is cumbersome
  - Good dynamic range
Motivation - III

- PWPM
  - Outphasing with combiner before PA
  - Use a single PA
  - Moderate dynamic range
Bandpass Pulse-Width Modulation - I

\[ f_0 = \frac{1}{T} \]

- \( \text{PWM Amp.} \propto \text{duty cycle} \)

\[ a_o = \frac{4}{\pi} \sin d\pi \]

\[ d = \frac{\tau}{T} \]

- \( \text{BPF} \rightarrow \text{remove harmonic content} \)
Pulse Width Modulator - I

- Envelope stored in “outphasing” angle
- Large angle $\rightarrow$ small envelope
- Small angle $\rightarrow$ large envelope
Pulse Width Modulator - I
Pulse Width Modulator - II
PWM Combiner - Clock RX

\[ \text{Out}^- \quad \text{M}_3 \quad \text{M}_4 \quad \text{Out}^+ \]

\[ \text{In}^+ \quad \text{M}_1 \quad \text{M}_2 \quad \text{In}^- \]

\[ \text{V}_x \quad \text{M}_5 \quad \text{M}_6 \quad \text{M}_7 \quad \text{M}_8 \]

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PWM Combiner - Buffer and Retiming

- Retiming every two stages
- 6 stages total
PWM Combiner – Diff NOR
PA Driver

Small Fan Out $\rightarrow$ Needed for narrow pulses
Class-E Power Amplifier - I

- $v_D$, $i_D$ shaped $\rightarrow$ minimal overlap
- Ideally ZVS
- Switch on $\rightarrow$ energy stored in $L_d$
- Switch off $\rightarrow$ energy transferred to output tank
Class-E Power Amplifier - II

- **Stress** – 
  \( v_D \sim 3.6V_{DD} \)

- **Occurs @ M\(_1\) off** → No “hot carrier” effect

- **Oxide Breakdown** → \( V_{DG} \) still large

- **Rule of thumb** → max \( V_{DG} < 2V_{DD,nom} \)

**Drain-Gate Max Voltage**

<table>
<thead>
<tr>
<th>Switch “On”</th>
<th>Switch “Off”</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.6V(_{DD})</td>
<td>( V_{DD,DR} )</td>
</tr>
</tbody>
</table>
Class-E Power Amplifier - III

- Cascode $\rightarrow$ Reduce stress per device
- Thick Gate I/O devices
- Finite supply inductor $\rightarrow$ reduced peak $v_D$ ($\sim 2.5V_{DD}$)

<table>
<thead>
<tr>
<th></th>
<th>Drain-Gate Max Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Switch “On”</strong></td>
<td><strong>Switch “Off”</strong></td>
</tr>
<tr>
<td>$M_2$</td>
<td>$V_B$</td>
</tr>
<tr>
<td>$M_1$</td>
<td>$V_{DD,DR}$</td>
</tr>
</tbody>
</table>

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Coarse Power Control

- 4 unit cells
- Coarse power control by disenabling path
- Switch layout optimized → Tradeoff R and C
PWPM PA Schematic

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Chip Microphotograph

- 65 nm Standard CMOS
- No UTM, No MIM
PA Characterization

4438C

Balun

\( \phi_1 \)

Combiner & PA

\( \phi_2 \)

Out+

Out-

Sense

Balun

4440A

Unit Buffer

Unit Buffer

\( x1 \)

\( x6 \)

3.5k\( \Omega \)

Sense

6pF
PA Output vs. Duty Cycle - I
PA Output vs. Duty Cycle - II

Coarse Power Control

Output Power (dBm)

PAE (%)
PA Output vs. Frequency

Output Power (dBm) vs. Frequency (GHz)

PAE (%) vs. Frequency (GHz)
PA Vector Signal Measurement
GMSK Modulated Signal

EVM=1.2% rms
Pout=27.5 dBm
PAE=25.3%
Spectral Mask
PA Envelope Correction

- Correction is offline
- Envelope ramp and measurement
- Correction $\rightarrow 6^{\text{th}}$ order polynomial fit
\(\pi/4\)-DQPSK Modulated Signal

EVM=4.6\% rms
Pout=26.7 dBm
PAE=21\%
## PA Summary

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>65nm, no UTM, no MIM</td>
</tr>
<tr>
<td>Pout - Peak (dBm)</td>
<td>28.6</td>
</tr>
<tr>
<td>PAE - Peak (%)</td>
<td>28.8</td>
</tr>
<tr>
<td>Frequency Range (GHz)</td>
<td>1.6 – 2.5</td>
</tr>
<tr>
<td>$P_{out}$ PWM (dBm)</td>
<td>21.6 – 28.6</td>
</tr>
<tr>
<td>$P_{out}$ PWM + Core Switching (dBm)</td>
<td>15.3 – 28.6</td>
</tr>
<tr>
<td>Voltage - Output Stage - (V)</td>
<td>2.5</td>
</tr>
<tr>
<td>Voltage - Driver &amp; Comb. - (V)</td>
<td>1.5</td>
</tr>
</tbody>
</table>
Conclusions

• A PWPM PA is introduced in 65nm CMOS
• The PA achieves a peak power of 28.6 dBm
• The PA with PWPM is suitable for applications of moderate peak-average (~6-10 dBm)