A Switched-Capacitor Power Amplifier for EER/Polar Transmitters

S.-M. Yoo, J.S. Walling, E.C. Woo, D.J. Allstot

University of Washington, Seattle, WA
Outline

• Motivation
• Switched-Capacitor PA
• Efficiency
• PA Design
• Measurement Results
• Conclusions
Need for High Average Efficiency

- PA power consumed in transmitter is huge
- High PAR in high-speed communication
  - WiMAX, LTE $\rightarrow$ OFDM modulation
- Switching PAs
  - Always saturated
  - 🎉 Good efficiency
  - 🙁 Need envelope restoration
Switching PA: EER and Outphasing

- **Outphasing**
  - Need 2 PAs
  - Combiner is cumbersome
  - Constant driver power consumption at backoff

- **EER**
  - Need DAC and supply modulator
  - Supply modulator limits efficiency & increases die area
Digitally-Modulated PA

PA based on digital modulation
[Kavousian, et al., ISSCC 2007]
[Presti, et al., JSSC 2009]

- DAC, supply modulator functions combined
  - No supply modulator: Higher efficiency and smaller area
- Multiple unit current-cell-based PAs as DAC
Current-Cell-Based PA

- Accuracy / Efficiency Tradeoff
  - Accurate current cell requires high $r_{out}$
    - Cascode or more voltage headroom: Lower efficiency
  - Extra resolution required for predistortion
  - Efficiency: $\eta_{ideal} = \frac{P_{out}}{P_{DC}} \propto \frac{P_{out}}{V_{out}} \propto \sqrt{P_{out}}$
Switched-Capacitor PA

- Capacitor can be arrayed
  - Single capacitor can be split into many capacitors
  - Each capacitor is connected to VDD or GND
  - Constant resonant frequency
  - High efficiency with linear envelope
Energy in Switched Capacitor

- Assume ideal source
- No energy loss
- Constant top-plate capacitance
Thevenin Equivalent Circuit

- Digitally-controlled output voltage
- Constant top-plate capacitance (NC) vs. the number of switched capacitors

$$Z_{Th} = \frac{1}{j\omega NC}$$
Output Power

\[ P_{\text{out}} \] delivered to \( R_{\text{OUT}} \)

- \( 4/\pi \) for fundamental frequency component
- Approximation with perfect filtering for high-order harmonics

\[
V_{\text{OUT}} = \frac{1}{2} \frac{4}{\pi} \frac{n}{N} V_{DD}
\]

\[
P_{\text{OUT}} = \frac{2n^2V_{DD}^2}{\pi^2 N^2 R}
\]
Power Dissipated in SC

- Charging & discharging with non-ideal switch → $CV^2f$ loss
- Assume sharp $t_r, t_f$ with constant current through $L$
- Series capacitance switched with envelope

\[
P_{SC} = C_{in}V_{DD}^2 f = \frac{n(N-n)}{N^2}CV_{DD}^2 f
\]
Ideal Efficiency

- Higher efficiency with higher $Q_{\text{Loaded}}$
- Higher $Q_{\text{Loaded}}$:
  - Smaller Capacitor
  - Less CV$^2$f loss
  - Limited efficiency due to L & switch

\[ \eta = \frac{P_{\text{OUT}}}{P_{\text{SC}} + P_{\text{OUT}}} = \frac{4n^2}{4n^2 + \frac{\pi n(N - n)}{Q_{\text{Loaded}}}} \]

\[ Q_{\text{Loaded}} = \frac{2\pi f L}{R} = \frac{1}{2\pi f CR} \]
Practical Efficiency

\[ \eta_{Ideal} = \frac{P_{OUT}}{P_{SC} + P_{OUT}} \]

\[ \eta = \frac{\alpha \cdot P_{OUT}}{P_{SC} + P_{OUT} + P_{SWC} + P_{DR} + P_{CLOCK}} \]

- Other efficiency losses
  - Lossy Inductor & SW R: \( \rightarrow \alpha \)
  - SW parasitic C: \( P_{SWC} = \frac{n}{N} C_{SW} V_{DD}^2 f \)
  - Switch driver: \( P_{DR} = \frac{n}{N} C_{DR} V_{DD}^2 f \)
  - Clock distribution: \( P_{CLOCK} = C_{CLOCK} V_{DD}^2 f \)
6-bit Switched-Capacitor Array

- Split into 4-bit unary and 2-bit binary arrays
- Additional bits available
  - More unary/binary bits or C-2C ladder
- Switch-driver can also be split
Switch Implementation

- Cascode $\Rightarrow$ More output power with same $R_{out}$
- Total supply voltage of 2*VDD
- Thin-gate devices
- Separate driver voltage ranges for NMOS & PMOS

[Stauth, et al., CICC 2008]
Switched-Capacitor PA Schematic

[Diagram of a switched-capacitor PA with various components labeled, including Vdd, 2Vdd, 0-Vdd, SW driver, selection logic, B1, B0, BA, B5-B2, B5-B0, and a binary-to-thermometer decoder.]
Chip Microphotograph

- 90 nm RF LP CMOS process (MIM cap and UTM)
PA Measurement: $P_{\text{out}}$ & PAE

- 6-bit implementation
- Less $P_{\text{driver}}$ at backoff
- $\eta_{\text{Peak}} = 45\%$, $\eta_{-6\text{dB}} = 29\%$
Non-ideal switch
Different impedance seen from source depending on input code
Peak $P_{out} \geq 23\text{dBm}$
Peak $\eta \geq 42\%$
• 64 QAM/OFDM
• EVM = 2.9%

• $P_{\text{out}} = 17.3$ dBm
**Envelope Linearity Before Predistortion**

- INL < ± 3 LSB, DNL < ± 0.5 LSB with 23dBm Peak $P_{out}$
- Robust predistortion with less nonlinearity
## PA Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>90nm CMOS</th>
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<tbody>
<tr>
<td>Resolution</td>
<td>6 bits</td>
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<tr>
<td>Supply Voltage (VDD, VDD2)</td>
<td>1.5V / 3.1V</td>
</tr>
<tr>
<td>Output Power (Peak/64 QAM OFDM)</td>
<td>25dBm / 17.7dBm</td>
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<tr>
<td>PAE (Peak/64 QAM OFDM)</td>
<td>45% / 28%</td>
</tr>
<tr>
<td>EVM (64 QAM OFDM)</td>
<td>2.9%</td>
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<tr>
<td>Frequency</td>
<td>1.8GHz – 2.8GHz</td>
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<tr>
<td>Die Area</td>
<td>1.04mm² (0.73mm×1.43mm)</td>
</tr>
</tbody>
</table>
## Performance Comparison

<table>
<thead>
<tr>
<th>Reference</th>
<th>Degani, et. al. ISSCC 2008</th>
<th>Presti, et. al. JSSC 2009</th>
<th>Xu, et. al. ESSCIRC 2010</th>
<th>Walling, et. al. JSSC 2009</th>
<th>This work</th>
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<tbody>
<tr>
<td>Architecture</td>
<td>Class-AB</td>
<td>DPA Current Cell</td>
<td>Outphasing</td>
<td>Class-G</td>
<td>Switched-Capacitor</td>
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<tr>
<td>Process</td>
<td>90nm</td>
<td>0.13um</td>
<td>32nm</td>
<td>0.13um</td>
<td>90nm</td>
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<tr>
<td>Peak Power</td>
<td>25 dBm</td>
<td>25 dBm</td>
<td>25.1 dBm</td>
<td>29.3 dBm</td>
<td>23.4 dBm</td>
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<tr>
<td>Peak Efficiency</td>
<td>50%</td>
<td>47%</td>
<td>40.6%</td>
<td>69%</td>
<td>42%</td>
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<tr>
<td>Avg. Power (OFDM)</td>
<td>15.5 dBm</td>
<td>15.3 dBm</td>
<td>18.6 dBm</td>
<td>19.6 dBm</td>
<td>17.3 dBm</td>
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<tr>
<td>Avg. Efficiency (OFDM)</td>
<td>19%</td>
<td>22%</td>
<td>18.1%</td>
<td>22.6%</td>
<td>28.4%</td>
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<td>Output Matching NW</td>
<td>N/A</td>
<td>Ext. Matching</td>
<td>On-Chip Balun</td>
<td>On-Chip Matching</td>
<td>On-Chip Matching</td>
</tr>
</tbody>
</table>
Conclusions

• First switched-capacitor PA
• Superior linearity in AM-AM
• Good backoff and average efficiency
• Eliminates supply voltage modulator that degrades efficiency & increases chip area
• Benefits from CMOS scaling