A 1.6 mW 5.4 GHz Transformer-Feedback \(g_m\)-Boosted Current-Reuse LNA in 0.18\(\mu\)m CMOS

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Abstract—Delivering high gain, low noise and good linearity simultaneously with low power consumption in fully-integrated CMOS low noise amplifiers (LNAs) has posed significant difficulty. This paper presents a 19 dB gain, 2.4 dB noise figure, common-gate common-source (CG-CS) single-ended LNA operating at 5.4 GHz. Using \(g_m\) boosting, current-reuse and transformer feedback techniques, the LNA mitigates several design issues seen in the widely used common-source-common-source current-reuse (CS-CS) LNAs and improves the IIP3 and reverse isolation of CG-CS schemes by 7 dB and 8 dB, respectively, while significantly reducing power consumption. Implemented in 0.18\(\mu\)m CMOS the LNA uses only 1.3 mA bias current from a 1.2V supply.

I. INTRODUCTION

In the RF receiver front-end low noise amplifiers (LNAs) are used to provide enough signal gain for overcoming noise in subsequent stages. They need to simultaneously satisfy, high gain, low noise and good linearity requirements while being power efficient. Differential LNAs provide higher gain and better distortion performance, but at the cost of increased area, power consumption and noise figure (NF) owing to lossy baluns. Amongst single-ended LNA topologies, current-reuse [1-4][9] LNAs (CRLNA) schemes have become good candidates for realizing high gain, low power and low noise, since they ‘re-use’ the same bias current in multiple gain stages providing ‘current-efficiency’. Common-source common-source (CS-CS) CRLNA [1,2] schemes have demonstrated these aforementioned benefits, but are plagued by complex frequency alignment of three LC resonant tanks, i.e. input, interstage and output resonant tanks, which is difficult to ensure over PVT variations. They also suffers from poor reverse isolation, which raises stability concerns at high gain operations. Recently, a CG-CS CRLNA [3,4] (Fig. 1(a)) has overcome these design issues achieving 20 dB gain and <3 dB NF with only 2.7 mW power consumption. The chief limitation of this design is reduced linearity, due to significant reduction in bias current and hence \(g_m\), of the CS stage. [4] proposes increasing the bias current of just the CS-stage (Fig. 1(a)) by introducing an additional current sinking transistor (\(M_3\)). It is shown that increasing the CS-stage current by 2 mA increases the IIP3 by 6 dB.

This paper enhances this design by providing an alternate way of achieving linearity improvement (Fig. 1(b)) without increasing the bias current. A passive transformer based negative feedback is used to enhance inductive degeneration of the LNA while simultaneously neutralizing of the parasitic gate-drain capacitance. This technique improves both linearity and reverse isolation without increasing bias current, noise or area. The proposed transformer-feedback current-reuse LNA (TF-CRLNA) operates at 5.4 GHz, achieves 19 dB gain, 2.4 dB NF, IIP3 of -14.2 dBm while consuming only 1.6 mW power. Section II presents the circuit topology and investigates the gain, linearity, reverse isolation and noise of a prototype. Section III presents the simulation results and the effects of transformer coupling, followed by conclusions.

II. \(g_m\)-BOOSTED TRANSFORMER FEEDBACK CURRENT RE-USE LNA

The proposed \(g_m\)-boosted CG-CS transformer-feedback current-reuse LNA (TF-CRLNA) schematic is shown in Fig. 1(b). The input stage of the LNA is a common gate (CG) stage which uses an on-chip spiral transformer with coupling ratio (\(k_1\)) and turns ratio (\(n_1\)) between gate and source input to boost the transconductance of the CG device [6]. The increased effective \(g_m\) implies smaller bias current needed for providing a wide-band 50\(\Omega\) match. The increased \(g_m\) also improves NF [3]. This stage is followed by an inductively-degenerated CS current re-use stage to provide higher overall gain and reverse isolation. The stages ac cascaded and the same dc bias current is used in both. The output of the first stage is fed to the gate of the second stage via a large dc-blocking capacitor. Both the output resonant tanks of the CG (\(L_1, C_1\)) and the CS stage (\(L_2, C_2\)) are tuned at \(f_0 = 5.4\) GHz.

A. Gain Analysis

Fig. 2 shows the equivalent circuit for the TF-CRLNA. Note that the intrinsic drain resistances, \(r_D\), is assumed large and omitted from the analysis. \(C_1\) and \(C_2\) comprise gate-source capacitance of \(M_1\) and total drain capacitance of \(M_2\), respectively. For ease of gain analysis the two ac-cascaded stages are separately evaluated. For the input stage the coupling ratio between the \(L_S\) and \(L_P\) inductors is \(k_1\), the mutual inductance (\(M_1\)) is equal to \(k_1\sqrt{L_S L_P}\) and the turns ratio \(n_1 = \sqrt{L_P/L_S}\).

Using nodal analysis the voltage gain \(V_2/V_1\) is derived and is shown in (1), where \(Y_{\text{in}} = \frac{1}{Z_{GS1}\|Z_{GD1}\|Z_{GS2} Z_{GD2}}\) and \(Z_{GS1}, Z_{GS2}, Z_{GD1}, Z_{GD2}\) are the impedances of \(C_{GS1}, C_{GS2}, C_{GD1}\) and \(C_{GD1}\) respectively. \(C_{GS1}\) and \(C_{GD1}\) are small due to reduced bias and \(g_m\) requirement for \(M_1\) transistor, following \(g_m\)-boosting. Neglecting these capacitances, \(A_{CG}\) reduces to

\[
A_{CG} = g_m(1 + k_1 n_1) Z_{L_1}\|Z_{C_1}. \quad (3)
\]
Transformer. Coupling coefficient of 0.2–0.8 can be typically where \( k = 1 \) is chosen to provide an amplifier (\( A - \)).

Simple inductively degenerated CS stage and (2) evaluates back and parasitic capacitance - the amplifier resolves to the \( k \) that for \( M \).

Linearity and Neutralization

Stage is designed for about 4-5 dB of gain. Both the load tanks \( dB \), is delivered by the more linear CG stage, while the CS derived is shown in (2), where \( M_2 = k_2 \sqrt{L_2 L_3}, n_2 = \sqrt{L_2} \), \( M_2/L_2 = k_2/n_2 \) and \( Z_L = Z_{L_2}||Z_{C_2} \). It is useful to note that for \( k_2 \) and \( C_{GD2} \) both zero, i.e., no transformer feedback and parasitic capacitance - the amplifier resolves to the simple inductively degenerated CS stage and (2) evaluates to \( -g_m Z_L l_1 \approx -Z_L l_1 \), as expected. The total gain of the amplifier (\( A_T \)) is the product of gains from the two stages, \( A_T = A_{CG} A_{CS} \). The majority of the power gain, about 14 dB, is delivered by the more linear CG stage, while the CS stage is designed for about 4-5 dB of gain. Both the load tanks \( Z_{L_1}||Z_{C_1} \) and \( Z_{L_2}||Z_{C_2} \) are designed to resonate at 5.4 GHz.

**B. Linearity and Neutralization**

The cascaded IIP3 of the two stage LNA is given by

\[
IIP3 = \frac{1}{\frac{1}{IIP_{ACG}} + \frac{1}{IIP_{ACS}}}.
\]

(4)

The CG stage is inherently more linear than the CS stage at the same bias current [6]. Also since \( G_{CG} \approx 14 \) in this case, it is clear from (4) that the IIP3 of the CS stage dominates the overall IIP3. For a small bias current the linearity of the amplifier is strongly limited by the low \( g_m \) of the \( M_2 \) device. To enhance the linearity of the CS stage an on-chip spiral transformer, comprising \( L_3 \) and the drain inductor \( L_2 \) is added. Originally used as a capacitive neutralization technique by Cassan [5], this work analyzes and extends the transformer feedback technique to linearity enhancement, particularly useful in a current-reuse LNA. The introduction of the transformer introduces bilateral signal flow in the CS-stage. Its role is two-fold:

1. **Linearity**: From (2) it can be derived that coupling from \( L_2 \) to \( L_3 \) increases the effective inductive degeneration of the CS-stage by a factor

\[
T \approx 1 + \frac{k_2 Z_{L_2}||Z_{C_2}}{n_2 Z_{L_3}}.
\]

At \( w_0 \), \( Z_{L_2} = Z_{C_2} \) and \( Z_{L_2}||Z_{C_2} = \frac{1}{2} Z_{L_2} \). Using \( n_2 = \sqrt{\frac{L_3}{L_2}} \), (5) simplifies to \( T \approx 1 + \frac{1}{2} k_2 n_2 \). Practical implementation
values for $T$ can lie between 1 and 2.5 without additional area overhead. The third-order harmonics of the amplifier output is attenuated by the cubic power of the negative feedback loop gain, $\approx (g_m Z_L T + 1)^3$. Thus this coupling significantly improves linearity of the amplifier compared to simple inductive degeneration schemes.

2) Neutralization: The coupling from $L_3$ to $L_2$ provides a feed-forward signal that increases gain (second term in the numerator of (2)). However, another feed-forward signal path exists due to the $C_{GD2}$, which reduces gain and reverse isolation (third term in the numerator (2)). Interestingly, these two feed-forward signals are opposing in nature, and by canceling the feed-forward signals from these two paths, neutralization of $C_{GD2}$, and thus increased reverse isolation, is achieved. To derive the condition of neutralization of the CS-stage the reverse signal flow graphs is derived and contributions of two paths are equaled, as shown in [5]. The two paths are neutralized when

$$\frac{n_2}{k_2} \approx \frac{C_{GS2}}{C_{GD2}}.$$  

(6)

We use this design choice to enable both neutralization of the gate-to-drain capacitance of M2, $C_{GD2}$, and enhanced inductive degeneration. The inductor $L_3$ is typically small and lies within the outer dimensions of $L_2$. Overall, when applied to current-reuse LNAs this scheme delivers high gain, improved reverse isolation and linearity with additional power, area or noise.

C. Noise Figure

The inductors and transformers are assumed to be lossless and contribute no noise. Friis equation is used to calculate the noise factor of the two ac-cascaded stages.

$$F = F_{CG} + \frac{F_{CS} - 1}{G_{CG}}.$$  

(7)

The noise factor for the two stages can be derived as

$$F_{CG} = 1 + \frac{\gamma}{\alpha g_m R_s (1 + n_3 k_1)}.$$

(8)

$$F_{CS} \approx 1 + \frac{\gamma}{1.5 \alpha g_m R_{out}} + \frac{\delta_{m}}{5 m} \frac{w}{w_T}.$$  

(9)

Here $R_s$ and $R_{out}$ are the source and output impedances. For $k_1 = 0.7$, $n_1 = 1$, $T = 1.75$, $w_T = 0.1$ and typical device parameters for 0.18 $\mu$m CMOS process ($\gamma = 2$, $\alpha = 0.85$, $\delta = 4$) the NF evaluates to 2.9 dB for the CG stage and 2.4 dB for the CS stage. Substituting these values and using $G_{CG} = 14$ dB in Friis equation (7) yields a NF of $\sim 3$ dB for the whole TF-CRLNA.

III. Simulation Results

The LNA is implemented in 0.18 $\mu$m 7-metal IBM RF CMOS process and biased with 1.3 mA of dc current from a 1.2 V supply for peak gain. The S-parameters are shown in Fig. 3. A wide-band input match with $S_{11} < -10$ dB was observed. Since the input match is determined by the input stage bias is set at 700 mV. The CS stage bias is changed from 0.8-1.2 V for increasing gain of 14-19 dB with NF varying between 2.4-3.8 dB. Due to low headroom design, the LNA can be operated over a 0.8-1.8 V supply range with gain and bias current ranging from 15.4-21 dB and 0.9-1.8 mA, respectively. A tapped-capacitor output gives good narrow-band output match of $S_{22} < -12$ dB. A maximum gain of 19 dB with reverse isolation of $> 40$ dB is observed. In this design the value of $\frac{C_{GS2}}{C_{GD2}}$, is $\sim 5$. Hence a transformer turns ratio of about 2.6 and coupling coefficient of 0.5 was initially chosen.

Fig. 4 shows the effect of $k_2$ on overall gain, noise and reverse isolation. An increase of 17 dB in reverse isolation is observed as $k_2$ is increased from $0$ to $0.8$, while gain drops only by $3$ dB and noise is largely unaffected. It is seen that for a fixed size of $L_3$, large $k_2$ reduces gain due to increased inductive degeneration and increases linearity. However a low $k_2$ gives inadequate neutralization of $C_{GD2}$. Hence a trade-off between gain, linearity and reverse isolation is made with $k_2$ being the key design variable. Increasing $L_3$ reduces the gain of the second stage. PVT variations can lead to $\sim$10% inductor and capacitor variations, while coupling coefficient remains largely constant. A small $L_3$ also makes frequency alignment of the two stages easier over PVT variations. Keeping these design trade-offs in mind, simulations yield a near optimal $k_2 = 0.4$ and $n_2 = 2.3$. The size of $L_3$ is determined as 300 pH, while that of $L_2$ is 1.6 nH.

An IIP3 of -14.1 dBm is observed (Fig. 5). Note that a higher $k_2$ could be used to further increase the IIP3 and meet IEEE 802.11a WLAN standards. Fig. 6 shows the noise figure of the LNA to be around 2.4 dB, which is somewhat better than our first-order theoretical calculations. Fig. 7 shows the layout of the LNA with total area (pads included) of 0.45 $mm^2$. Table-I shows the performance of the LNA and compares it to recently published CRLNAs. It improves the linearity of the LNA in [3,4] by about 7 dB. The reverse isolation is improved by 8 dB when compared to no transformer feedback case. Note that these enhancements are achieved while further reducing power consumption and meeting all key performance parameters. The LNA is unconditionally stable with a $k$-factor $\gg 10$. The popular LNA figure of merit (FoM) (dB) used here is given by

$$FoM = -NF + IIP3 + G - 10 \log_{10} \frac{P_{dc}}{1 mW} + 20 \log_{10} \frac{w_0}{2 \pi 10^{6} H z}.$$  

(10)

The LNA achieves the lowest power consumption of 1.6 mW and highest FoM merit of 14 amongst comparable works.

IV. Conclusion

This paper applies a transformer feedback based neutralization technique in a $g_m$-boosted current-reuse fully-integrated CG-CS LNA. Enhanced linearity and reverse isolation without increasing bias current or area is demonstrated. A single-ended prototype of this LNA implemented in 0.18 $\mu$m CMOS demonstrates 2.4 dB NF, 19 dB gain and $> 40$ dB reverse isolation while consuming only 1.6 mW of power. To our knowledge, this is one of the lowest power consumption >
Fig. 3. Scattering parameters of the proposed LNA vs frequency.

Fig. 4. Effect of \( k_2 \) on noise figure, gain and reverse isolations.

5 GHz current-reuse LNA reported till date, at comparable performance.

REFERENCES


Table 1

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